



STF13NM60N-H

N-channel 600 V, 0.28 Ω , 11 A MDmesh™ II Power MOSFET
in TO-220FP

Features

Type	V _{DSS} (@T _{jmax})	R _{DS(on)} max	I _D
STF13NM60N-H	650 V	< 0.36 Ω	11 A

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance

Application

- Switching applications

Description

This series of devices implements second generation MDmesh™ technology. This revolutionary Power MOSFET associates a new vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. It is therefore suitable for the most demanding high efficiency converters.

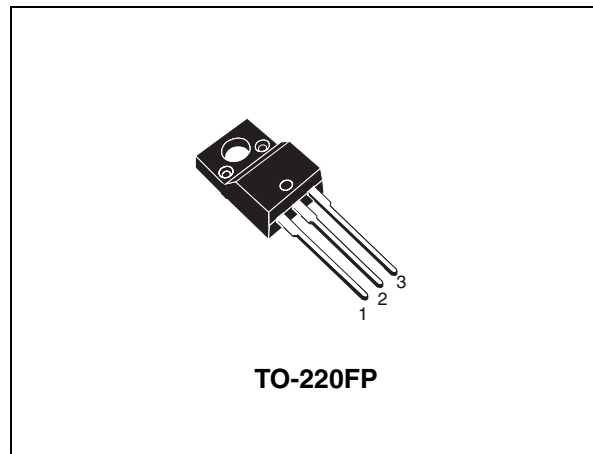


Figure 1. Internal schematic diagram

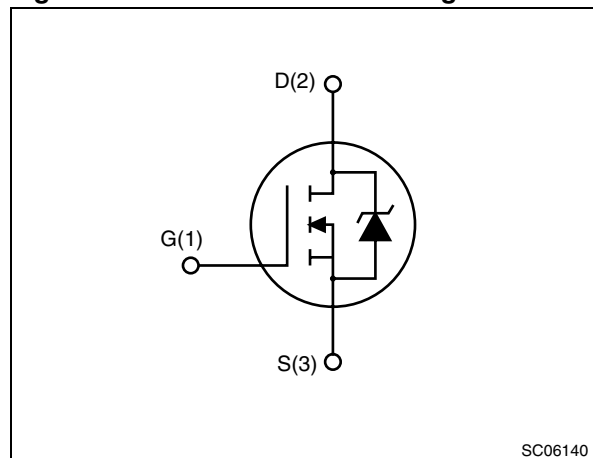


Table 1. Device summary

Order codes	Marking	Packages	Packaging
STF13NM60N-H ⁽¹⁾	13NM60N	TO-220FP	Tube

1. The device meets ECOPACK® standards, an environmentally-friendly grade of products commonly referred to as "halogen-free". See [Section 4: Package mechanical data](#).

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage ($V_{GS} = 0$)	600	V
V_{GS}	Gate-source voltage	± 25	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	11 ⁽¹⁾	A
I_D	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	6.93 ⁽¹⁾	A
$I_{DM}^{(2)}$	Drain current (pulsed)	44 ⁽¹⁾	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	25	W
$dv/dt^{(3)}$	Peak diode recovery voltage slope	15	V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink ($t=1\text{ s}; T_C=25\text{ }^\circ\text{C}$)	2500	V
T_{stg}	Storage temperature	-55 to 150	$^\circ\text{C}$
T_j	Max. operating junction temperature	150	$^\circ\text{C}$

1. Limited only by maximum temperature allowed
2. Pulse width limited by safe operating area
3. $I_{SD} \leq 11\text{ A}$, $di/dt \leq 400\text{ A}/\mu\text{s}$, $V_{DD} \leq 80\% V_{(BR)DSS}$

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	5	$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient max	62.5	$^\circ\text{C}/\text{W}$
T_l	Maximum lead temperature for soldering purpose	300	$^\circ\text{C}$

Table 4. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AS}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_j max)	3.5	A
E_{AS}	Single pulse avalanche energy (starting $T_j=25\text{ }^\circ\text{C}$, $I_D=I_{AS}$, $V_{DD}=50\text{ V}$)	200	mJ

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	I _D = 1 mA, V _{GS} = 0	600			V
dv/dt ⁽¹⁾	Drain source voltage slope	V _{DD} =480 V, I _D = 9 A, V _{GS} =10 V		45		V/ns
I _{DSS}	Zero gate voltage drain current (V _{GS} = 0)	V _{DS} = Max rating V _{DS} = Max rating, @125 °C			1 10	μA μA
I _{GSS}	Gate-body leakage current (V _{DS} = 0)	V _{GS} = ± 20 V			0.1	μA
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 250 μA	2	3	4	V
R _{DS(on)}	Static drain-source on resistance	V _{GS} = 10 V, I _D = 5.5 A		0.28	0.36	Ω

1. Characteristic value at turn off on inductive load

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g _{fs} ⁽¹⁾	Forward transconductance	V _{DS} =15 V, I _D = 5.5 A	-	7	-	S
C _{iss} C _{oss} C _{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V _{DS} = 50 V, f = 1 MHz, V _{GS} = 0	-	790 60 3.6	-	pF pF pF
C _{oss eq.} ⁽²⁾	Equivalent output capacitance	V _{GS} = 0, V _{DS} = 0 to 480 V	-	135	-	pF
Q _g Q _{gs} Q _{gd}	Total gate charge Gate-source charge Gate-drain charge	V _{DD} = 480 V, I _D = 11 A, V _{GS} = 10 V, <i>(see Figure 17)</i>	-	30 15 4	-	nC nC nC
R _G	Gate input resistance	f=1 MHz Gate DC Bias=0 Test signal level = 20 mV open drain	-	4.7	-	Ω

1. Pulsed: Pulse duration = 300 μs, duty cycle 1.5%

2. C_{oss eq.} is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DS}

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300\text{ V}$, $I_D = 5.5\text{ A}$ $R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$ (see Figure 16)		3		ns	
t_r	Rise time			8		ns	
$t_{d(off)}$	Turn-off delay time				30		ns
t_f	Fall time				10		ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
I_{SD}	Source-drain current		-		11	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				44	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 11\text{ A}$, $V_{GS} = 0$	-		1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 9\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 100\text{ V}$ (see Figure 18)	-	230		ns
Q_{rr}	Reverse recovery charge			2		μC
I_{RRM}	Reverse recovery current			18		A
t_{rr}	Reverse recovery time	$I_{SD} = 9\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 100\text{ V}$, $T_j = 150\text{ }^\circ\text{C}$ (see Figure 18)	-	290		ns
Q_{rr}	Reverse recovery charge			190		μC
I_{RRM}	Reverse recovery current			17		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

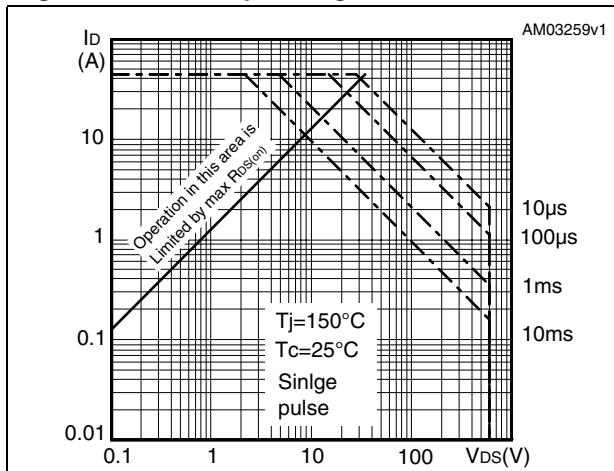


Figure 3. Thermal impedance

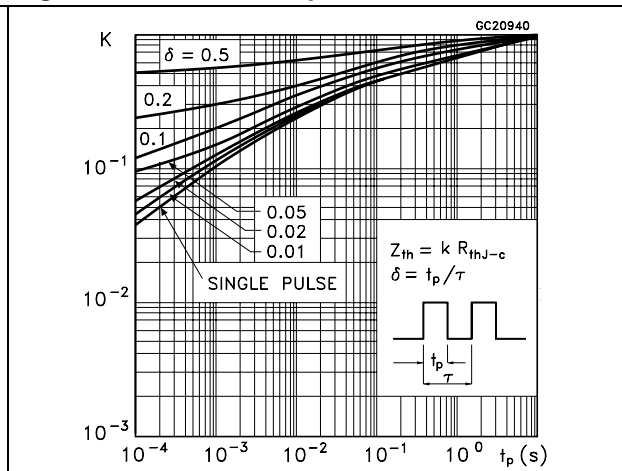


Figure 4. Safe operating area for DPAK

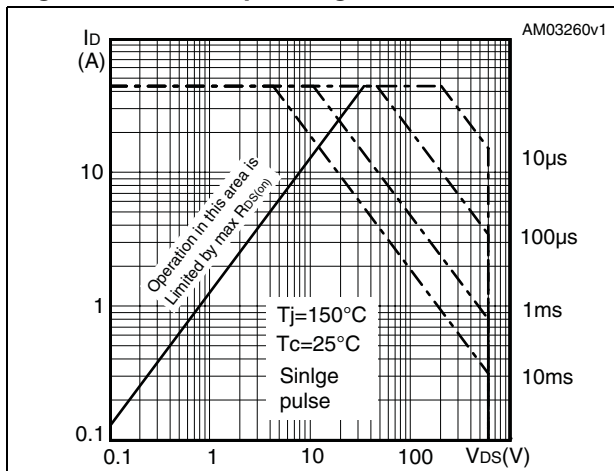


Figure 5. Thermal impedance for DPAK

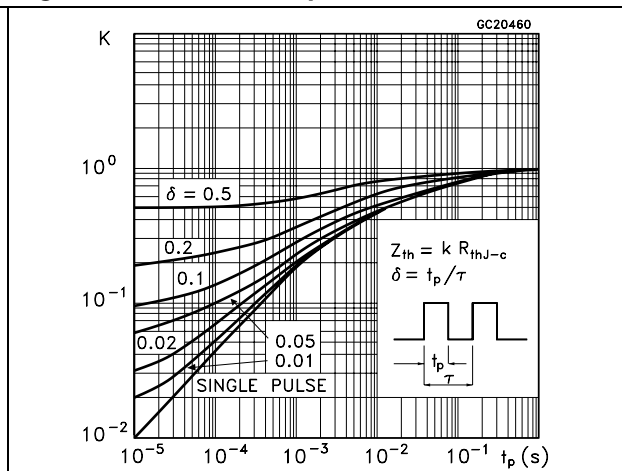


Figure 6. Output characteristics

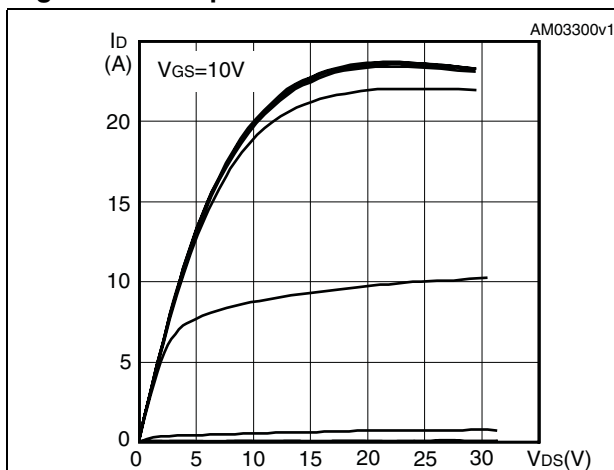


Figure 7. Transfer characteristics

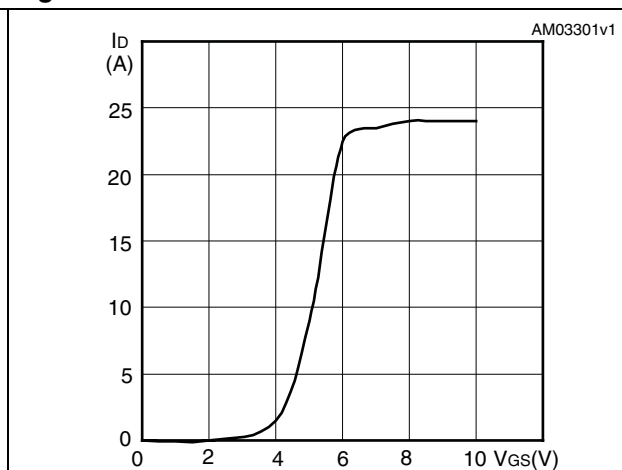


Figure 8. Transconductance

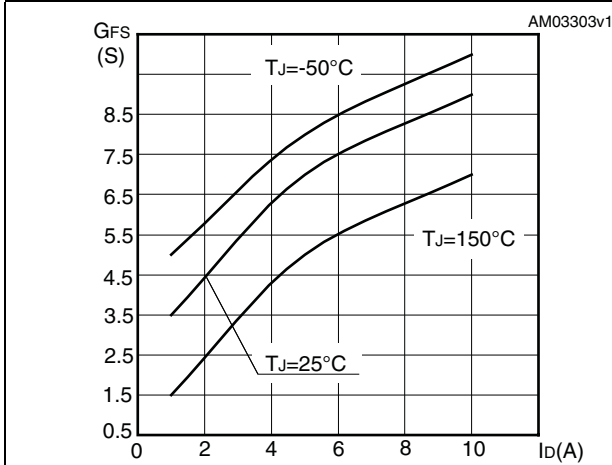


Figure 9. Static drain-source on resistance

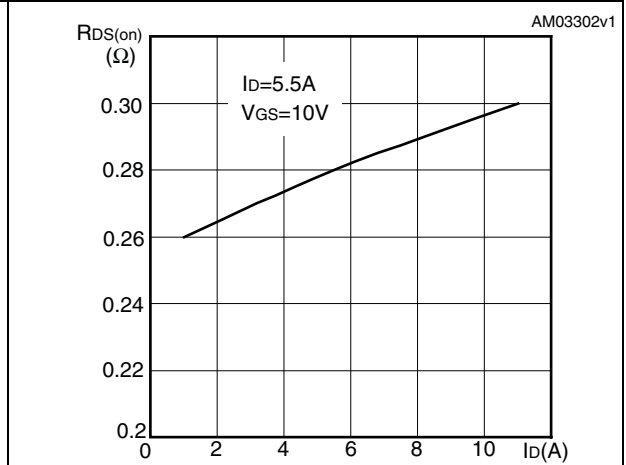


Figure 10. Gate charge vs gate-source voltage

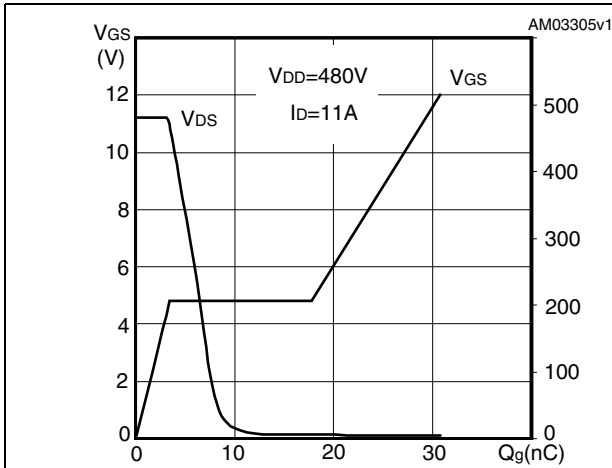


Figure 11. Capacitance variations

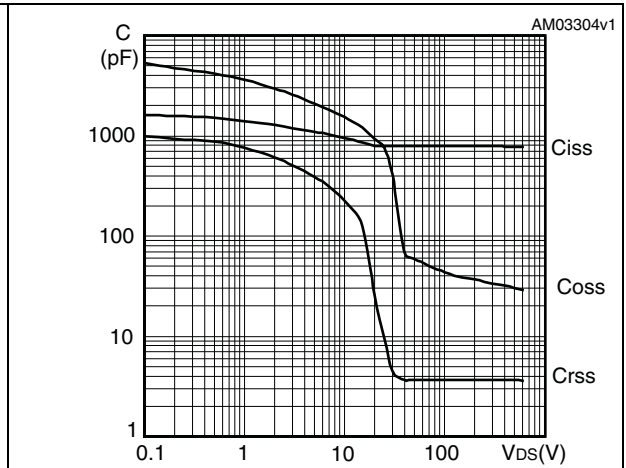


Figure 12. Normalized gate threshold voltage vs temperature

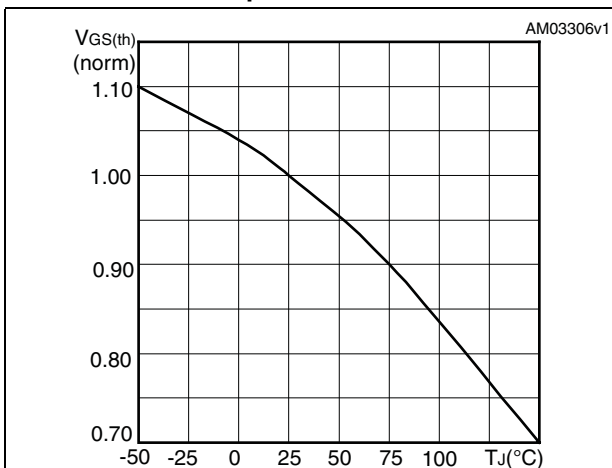


Figure 13. Normalized on resistance vs temperature

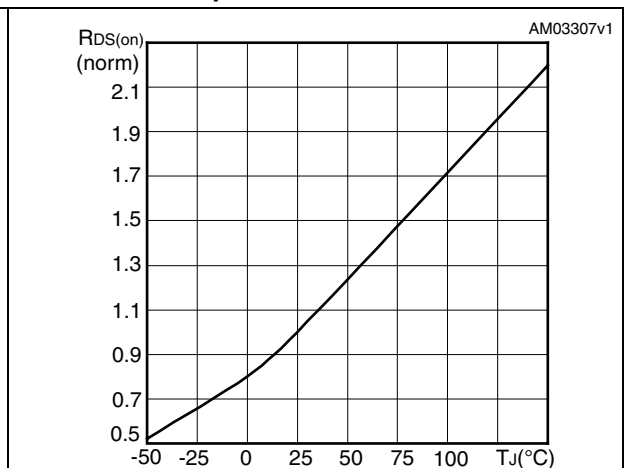


Figure 14. Source-drain diode forward characteristics

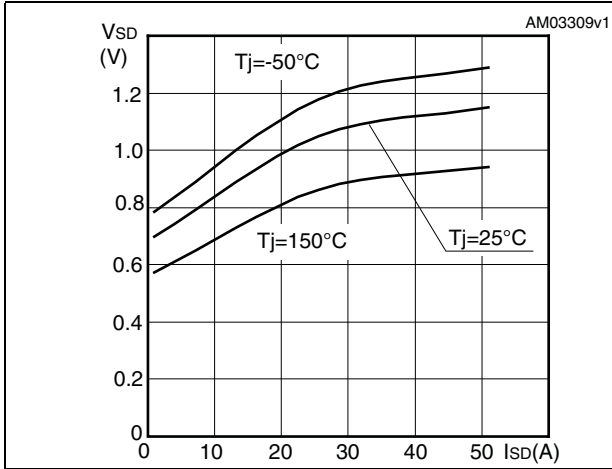
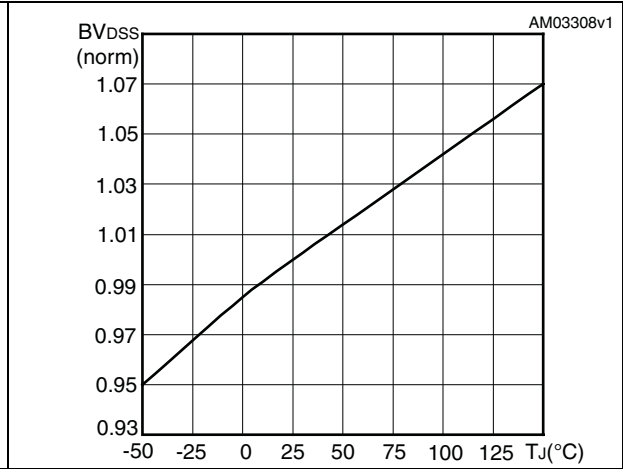


Figure 15. Normalized B_{VDS} vs temperature



3 Test circuits

Figure 16. Switching times test circuit for resistive load

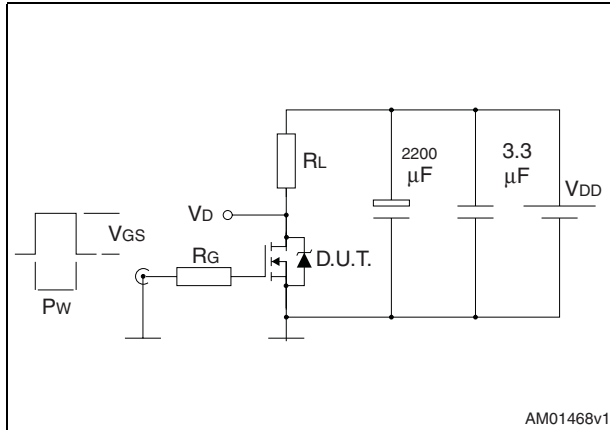


Figure 17. Gate charge test circuit

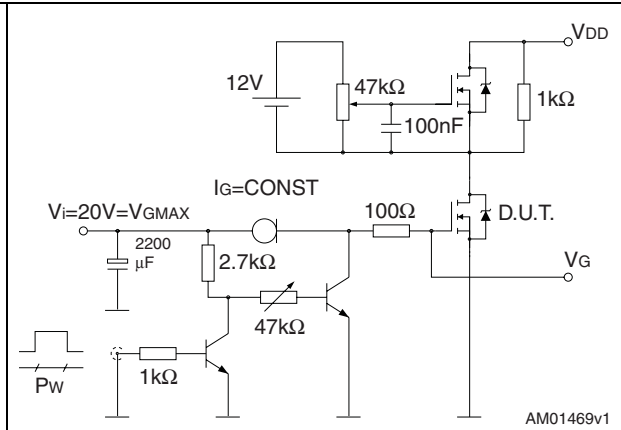


Figure 18. Test circuit for inductive load switching and diode recovery times

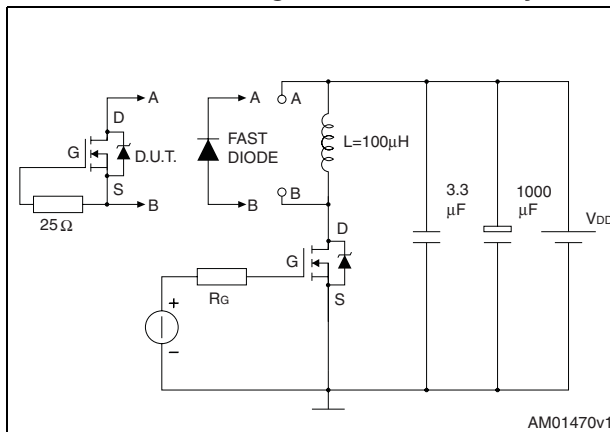


Figure 19. Unclamped inductive load test circuit

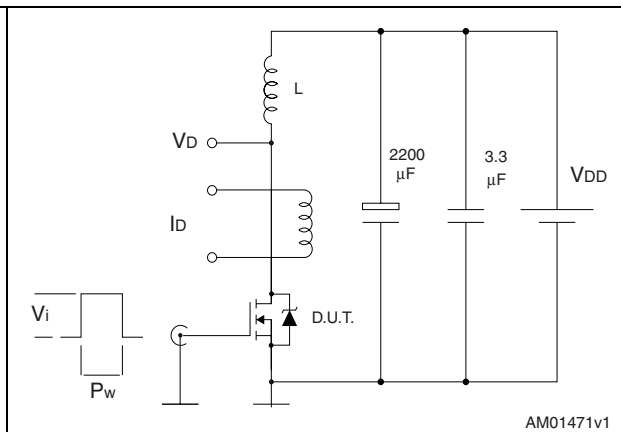


Figure 20. Unclamped inductive waveform

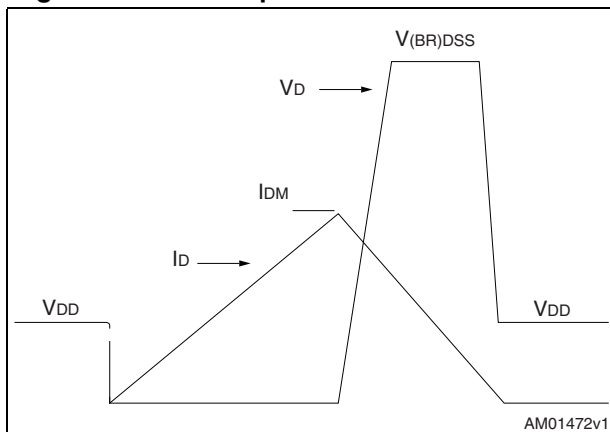
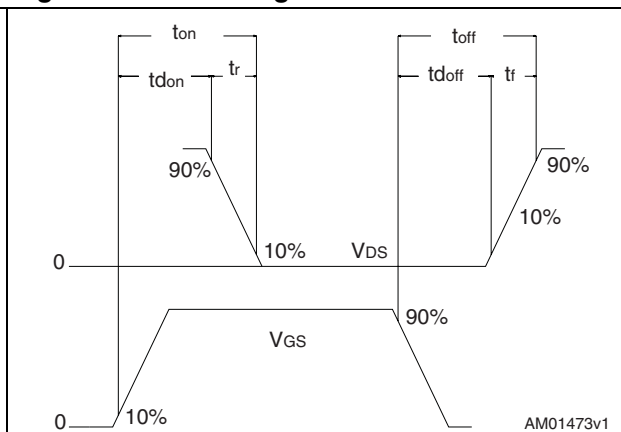


Figure 21. Switching time waveform



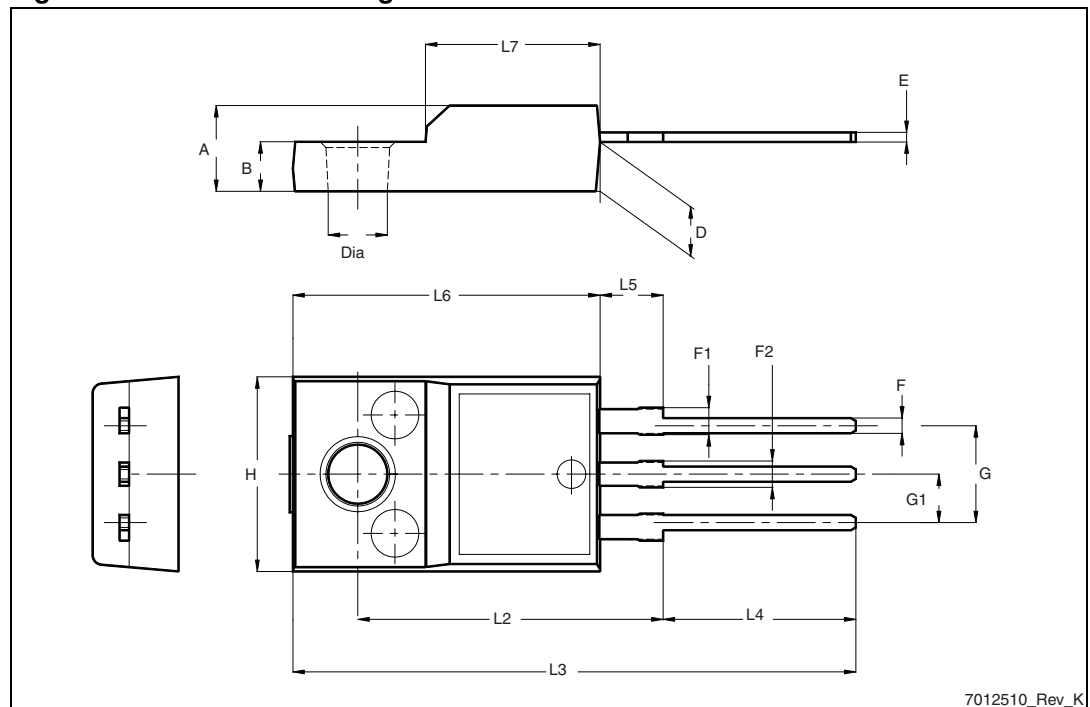
4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 9. TO-220FP mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

Figure 22. TO-220FP drawing



5 Revision history

Table 10. Document revision history

Date	Revision	Changes
08-Jan-2010	1	First release

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