Two-Phase PWM Controller for Graphics Processor Units (GPU)

Increase in GPU clock frequency is accompanied by associated increase in the demand for power and transient-current slew rate. At the same time, the voltage tolerance requirement during steady-state and transient operation is becoming more stringent of advanced GPU. The ISL9502 is a two-phase PWM controller with embedded gate drivers, which is tailored to meet the power and dynamic requirements. The two-phase buck converter uses two interleaved channels to effectively double the output voltage ripple frequency and thereby reduce output voltage ripple amplitude with fewer components, lower component cost, reduced power dissipation, and smaller real estate area.

The heart of the ISL9502 is the patented R3 (Robust Ripple Regulator®) modulator. Compared with the traditional multi-phase buck regulator, R3 technology has the fastest transient response. This is due to the R3 modulator commanding variable switching frequency during a load transient.

At heavy load operation of the active mode, ISL9502 commands the two phase continuous conduction mode (CCM) operation. While the pin SET3 is asserted at the medium or light load, the ISL9502 smoothly disables one phase and operates in a one-phase operation. Once in one-phase operation, when the GPU further lowers the load current, the ISL9502 enables diode emulation to maximize efficiency at light load depending on the logic of SET1 and SET2.

A 6-bit digital-to-analog converter (DAC) allows dynamic adjustment of the output voltage from 0.500V to 1.500V with 25mV step. A 0.5% system accuracy of the core output voltage over temperature is achieved by the ISL9502.

A unity-gain differential amplifier is provided for remote GPU die sensing. This allows the voltage on the GPU die to be accurately measured and regulated. Current sensing can be realized using either lossless inductor DCR sensing or precision resistor sensing. A single NTC thermistor network can thermally compensates the gain and the time constant of the DCR variations. Droop control, also referred as adaptive voltage positioning (AVP), is implemented in ISL9502 to reduce output decoupling capacitors and achieve more cost-effective transient-load regulation.

Features

- Precision Two-phase Buck PWM controller
  - 0.5% System Accuracy Over Temperature
  - Active Voltage Positioning Capability

- Internal Gate Driver with 2A Driving Capability

- Superior Load Transient Response

- Dynamic Phase Adding/Dropping

- Voltage Selection Input
  - 6-Bit VSEL Input
  - 0.500V to 1.500V in 25mV Steps
  - Supports VSEL Change On-The-Fly

- Multiple Current-Sensing Schemes Supported
  - Lossless Inductor DCR Current Sensing
  - Precision Resistive Current Sensing

- Thermal Monitor

- User Programmable Switching Frequency

- Differential Remote GPU Voltage Sensing

- Static and Dynamic Current Sharing

- Overvoltage, Undervoltage, and Overcurrent Protection

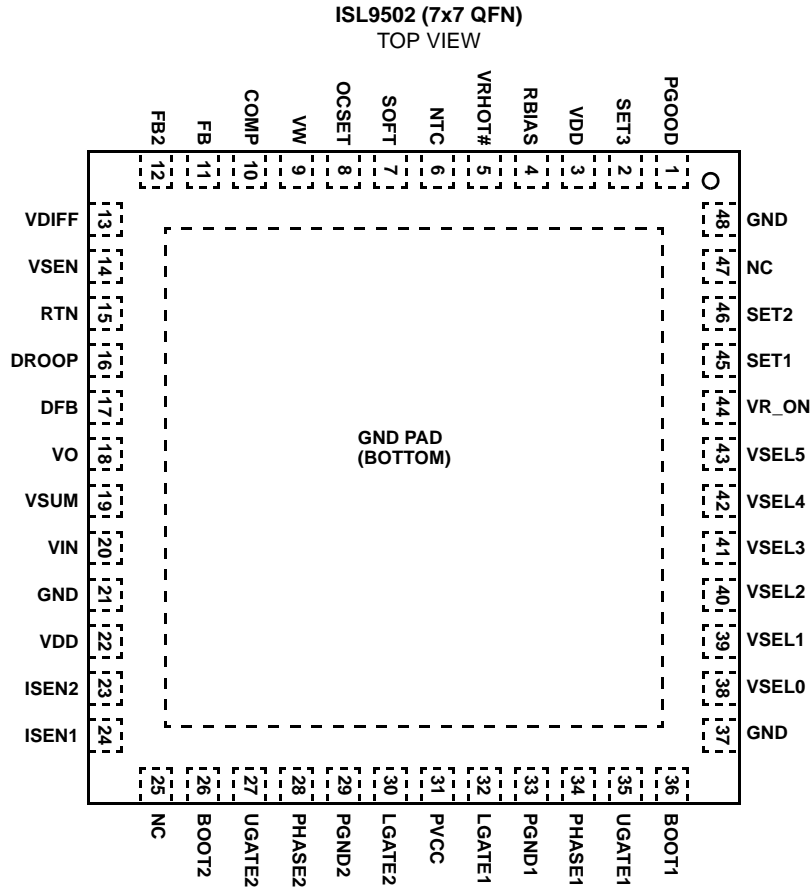- Pb-Free Plus Anneal Available (RoHS Compliant)

Ordering Information

PART NUMBER	PART MARKING	TEMP. (°C)	PACKAGE	PKG. DWG. #
ISL9502CRZ (Note)	ISL9502CRZ	-10 to 100	48 Ld 7x7 QFN (Pb-free)	L48.7x7
ISL9502CRZ-T (Note)	ISL9502CRZ	-10 to 100	48 Ld 7x7 QFN (Pb-free)	L48.7x7

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Pinout

ISL9502 (7x7 QFN)
TOP VIEW

Pin	Name
12	FB2
11	FB
10	COMP
9	VW
8	OCSET
7	SOFT
6	NTC
5	VRHOT#
4	RBIAS
3	VDD
2	SET3
1	PGOOD

Name	Pin
VDIFF	13
VSEN	14
RTN	15
DROOP	16
DFB	17
VO	18
VSUM	19
VIN	20
GND	21
VDD	22
ISEN2	23
ISEN1	24

GND PAD (BOTTOM)

Pin	Name
48	GND
47	NC
46	SET2
45	SET1
44	VR_ON
43	VSEL5
42	VSEL4
41	VSEL3
40	VSEL2
39	VSEL1
38	VSEL0
37	GND

Pin	Name
25	NC
26	BOOT2
27	UGATE2
28	PHASE2
29	PGND2
30	LGATE2
31	PVCC
32	LGATE1
33	PGND1
34	PHASE1
35	UGATE1
36	BOOT1

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Absolute Maximum Ratings

Supply Voltage, VDD . . . . -0.3 -+7V
Input Voltage, VIN . . . . +25V
Boot1,2 and UGATE1,2 . . . . +30V
ALL Other Pins. . . . . -0.3V to (VDD +0.3V)
Open Drain Outputs, PGOOD, VRHOT#. . . . . -0.3 -+7V

Recommended Operating Conditions

Supply Voltage, VDD . . . . +5V ±5%
Input Voltage, VIN . . . . +5V to 22V
Ambient Temperature. . . . . -10°C to 100°C
Junction Temperature . . . . -10°C to 125°C

Thermal Information

Thermal Resistance (Typical)	θ_{JA}°C/W	θ_{JC}°C/W
QFN Package (Notes 1, 2).	29	4.5

Maximum Junction Temperature . . . . 150°C
Maximum Storage Temperature Range. . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . 300°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.

2. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications V_{DD} = 5V, T_A = -10°C to 100°C, Unless Otherwise Specified.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
INPUT POWER SUPPLY						
+5V Supply Current	I_{VDD}	VR_ON = 3.3V	-	3.1	3.6	mA
		VR_ON = 0V	-	-	1	µA
Input Supply Current at VIN Pin	I_{VIN}	VR_ON = 0V, VIN = 25V,	-	-	1	µA
POR (Power-On Reset) Threshold	POR_r	V_{DD} Rising	-	4.35	4.5	V
	POR_f	V_{DD} Falling	3.9	4.1	-	V
SYSTEM AND REFERENCES						
System Accuracy	%Error (V_{cc_core})	No load, closed loop, active mode, T_A = 0°C to 100°C, VSEL = 0.75-1.5V	-0.5	-	0.5	%
		VSEL = 0.5-0.725V	-2	-	2	%
RBIAS Voltage	R_{RBIAS}	R_{RBIAS} = 147kΩ	1.45	1.47	1.49	V
Boot Voltage	V_{BOOT}		1.188	1.2	1.212	V
Maximum Output Voltage	V_{CC_CORE} (max)	VSEL = [000000]	-	1.5	-	V
	V_{CC_CORE} (min)	VSEL = [101000]	-	0.5	-	V
CHANNEL FREQUENCY						
Nominal Channel Frequency	f_{SW}	R_{FSET} = 3.9kΩ, 2 channel operation, V_{comp} = 2V	-	300	-	kHz
Adjustment Range			200	-	500	kHz
AMPLIFIERS						
Droop Amplifier Offset			-0.3	-	0.3	mV
Error Amp DC Gain	A_{V0}		-	90	-	dB
Error Amp Gain-Bandwidth Product	GBW	C_L = 20pF	-	18	-	MHz
Error Amp Slew Rate	SR	C_L = 20pF	-	5	-	V/µs
FB Input Current	$I_{IN(FB)}$		-	10	150	nA

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Electrical Specifications V_{DD} = 5V, T_A = -10°C to 100°C, Unless Otherwise Specified. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
ISEN						
Imbalance Voltage			-	-	1	mV
Input Bias Current			-	20	-	nA
SOFT-START CURRENT						
Soft-Start Current	I_{SS}		-46	-41	-36	µA
GATE DRIVER DRIVING CAPABILITY						
UGATE Source Resistance	$R_{SRC(UGATE)}$	500mA Source Current	-	1	1.5	Ω
UGATE Source Current	$I_{SRC(UGATE)}$	V_{UGATE_PHASE} = 2.5V	-	2	-	A
UGATE Sink Resistance	$R_{SNK(UGATE)}$	500mA Sink Current	-	1	1.5	Ω
UGATE Sink Current	$I_{SNK(UGATE)}$	V_{UGATE_PHASE} = 2.5V	-	2	-	A
LGATE Source Resistance	$R_{SRC(LGATE)}$	500mA Source Current	-	1	1.5	Ω
LGATE Source Current	$I_{SRC(LGATE)}$	V_{LGATE} = 2.5V	-	2	-	A
LGATE Sink Resistance	$R_{SNK(LGATE)}$	500mA Sink Current	-	0.5	0.9	Ω
LGATE Sink Current	$I_{SNK(LGATE)}$	V_{LGATE} = 2.5V	-	4	-	A
UGATE to PHASE Resistance	$R_{P(UGATE)}$		-	1.1	-	kΩ
GATE DRIVER SWITCHING TIMING (refer to timing diagram)						
UGATE Rise Time	t_{RU}	PV_{CC} = 5V, 3nF Load	-	8.0	-	ns
LGATE Rise Time	t_{RL}	PV_{CC} = 5V, 3nF Load	-	8.0	-	ns
UGATE Fall Time	t_{FU}	PV_{CC} = 5V, 3nF Load	-	8.0	-	ns
LGATE Fall Time	t_{FL}	PV_{CC} = 5V, 3nF Load	-	4.0	-	ns
UGATE Turn-on Propagation Delay	t_{PDHU}	PV_{CC} = 5V, Outputs Unloaded	20	30	44	ns
LGATE Turn-on Propagation Delay	t_{PDHL}	PV_{CC} = 5V, Outputs Unloaded	7	15	30	ns
BOOTSTRAP DIODE						
Forward Voltage		PV_{CC} = 5V, Forward Bias Current = 2mA	0.43	0.58	0.67	V
Leakage		V_R = 16V	-	-	1	µA
POWER GOOD and PROTECTION MONITOR						
PGOOD Low Voltage	V_{OL}	I_{PGOOD} = 4mA	-	0.11	0.4	V
PGOOD Leakage Current	I_{OH}	P_{GOOD} = 3.3V	-1	-	1	µA
Overvoltage Threshold	O_{VH}	V_O rising above setpoint > 1ms	160	200	240	mV
Severe Overvoltage Threshold	O_{VHS}	V_O rising above setpoint > 0.5µs	1.675	1.7	1.725	V
OCSET Reference Current		I(Rbias) = 10µA	9.8	10	10.2	µA
OC Threshold Offset		DROOP rising above OCSET > 120µs	-3.5	-	3.5	mV
Current Imbalance Threshold		Difference between ISEN1 and ISEN2 > 1ms	-	7.5	-	mV
Undervoltage Threshold	UV_f	V_O falling below setpoint for > 1ms	-360	-300	-240	mV
LOGIC INPUTS						
VR_ON and SET1 Inputs Low	V_{IL}		-	-	1	V
VR_ON and SET1 Inputs High	V_{IH}		2.3	-	-	V
Leakage Current of VR_ON	$I_{IL(3.3)}$	Logic input is low	-1	0	-	µA
	$I_{IH(3.3)}$	Logic input is high at 3.3V	-	0	1	µA

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Electrical Specifications V_{DD} = 5V, T_A = -10°C to 100°C, Unless Otherwise Specified. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Leakage Current of SET1	I_{IL_SET1}	SET1 input is low	-1	0	-	µA
	I_{IH_SET1}	SET1 input is high at 3.3V	-	0.45	1	µA
DAC(VSEL0-VSEL5), SET3 and SET2 Inputs Low	V_{IL}		-	-	0.3	V
DAC(VSEL0-VSEL5), SET3 and SET2 Inputs High	V_{IH}		0.7	-	-	V
Leakage Current of DAC(VSEL0-VSEL5), SET3 and SET2	I_{IL}	Logic input is low	-1	0	-	µA
	I_{IH}	Logic input is high at 1V	-	0.45	1	µA
THERMAL MONITOR						
NTC Source Current		NTC = 1.3 V	53	60	67	µA
Over-temperature Threshold		V(NTC) falling	1.165	1.18	1.2	V
VRHOT# Low Output Resistance	R_{HOT}	I = 20mA	-	5	9	Ω

ISL9502 Gate Driver Timing Diagram
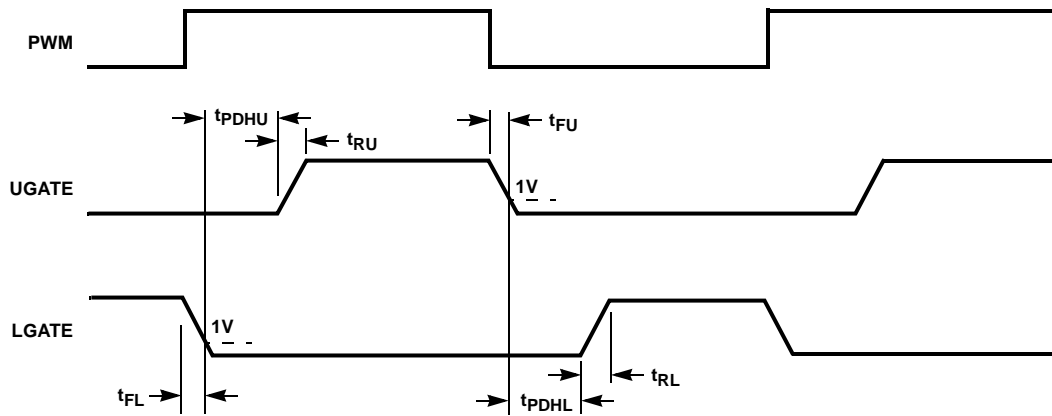
Functional Pin Description

PGOOD - Power good open-drain output. Will be pulled up externally by a 680Ω resistor to VCCP or 1.9kΩ to 3.3V.

SET3 - Low load current indicator input. When asserted low, indicates a reduced load-current condition, and product goes into single phase operation.

VDD - 5V control power supply.

RBIAS - 147kΩ resistor to GND sets internal current reference.

VRHOT# - Thermal overload output indicator with open-drain output. Over- temperature pull-down resistance is 10Ω.

NTC - Thermistor input to VRHOT# circuit and a 60µA current source is connected internally to this pin.

SOFT - A capacitor from this pin to GND pin sets the maximum slew rate of the output voltage. The SOFT pin is the non-inverting input of the error amplifier.

OCSET - Over-current set input. A resistor from this pin to VO sets DROOP voltage limit for OC trip. A 10µA current source is connected internally to this pin.

VW - A resistor from this pin to COMP programs the switching frequency (exa. 4.42kΩ ≅ 300kHz).

COMP - This pin is the output of the error amplifier.

FB - This pin is the inverting input of error amplifier.

FB2 - There is a switch between FB2 pin and the FB pin. The switch is closed in single-phase operation and is opened in two phase operation. The components connecting to FB2 is to adjust the compensation in single phase operation to achieve optimum performance if needed.

VDIFF - This pin is the output of the differential amplifier.

VSEN - Remote core voltage sense input.

RTN - Remote core voltage sense return.

DROOP - Output of the droop amplifier. The voltage level on this pin is the sum of Vo and the programmed droop voltage by the external resistors.

DFB - Inverting input to droop amplifier.

VO - An input to the IC that reports the local output voltage.

VSUM - This pin is connected to the summing junction for current sensing.

VIN - Supply voltage. It is used for input voltage feedforward to improve the input line transient performance.

GND - Signal ground. Connect to local controller ground.

VDD - 5V control power supply.

ISEN2 - Individual current sharing sensing for channel 2.

ISEN1 - Individual current sharing sensing for channel 1.

NC - Not connected. Connecting this pin to the ground.

BOOT2 - Upper gate driver supply voltage for phase 2. An internal boot strap diode is connected to the PVCC pin.

UGATE2 - Upper MOSFET gate signal for phase 2.

PHASE2 - Channel-2 phase. This pin should connect to the source of upper MOSFET.

PGND2 - Return path of the lower gate driver for phase 2.

LGATE2 - Lower-side MOSFET gate signal for phase 2.

PVCC - 5V power supply for gate drivers.

LGATE1 - Lower-side MOSFET gate signal for phase 1.

PGND1 - Return path of the lower gate driver for phase 1.

PHASE1 - Channel-1 phase. This pin should connect to the source of upper MOSFET.

UGATE1 - Upper MOSFET gate signal for phase 1.

BOOT1 - Upper gate driver supply voltage for phase 1. An internal boot strap diode is connected to the PVCC pin.

GND - Signal ground. Connect to local controller ground.

VSEL0, VSEL1, VSEL2, VSEL3, VSEL4, VSEL5 - Voltage selection input with VSEL0 is the least significant bit (LSB) and VSEL5 is the most significant bit (MSB).

VR_ON - Digital input enable. A high level logic signal on this pin enables the regulator.

SET1, SET2 - Select power-saving modes.

NC - Not connected.

GND - Signal ground. Connect to local controller ground.
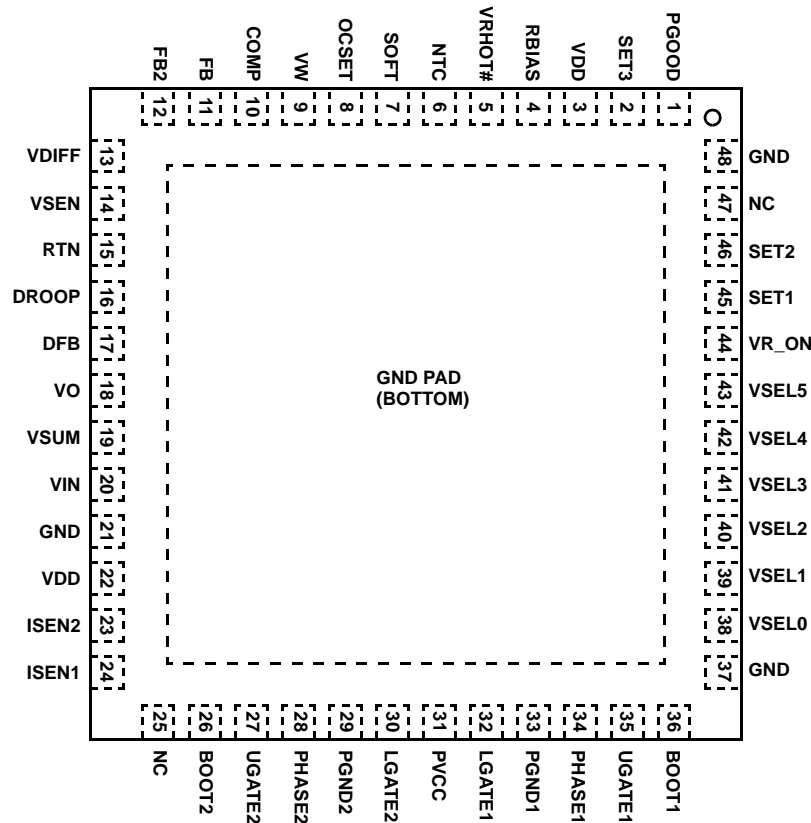
Functional Block Diagram
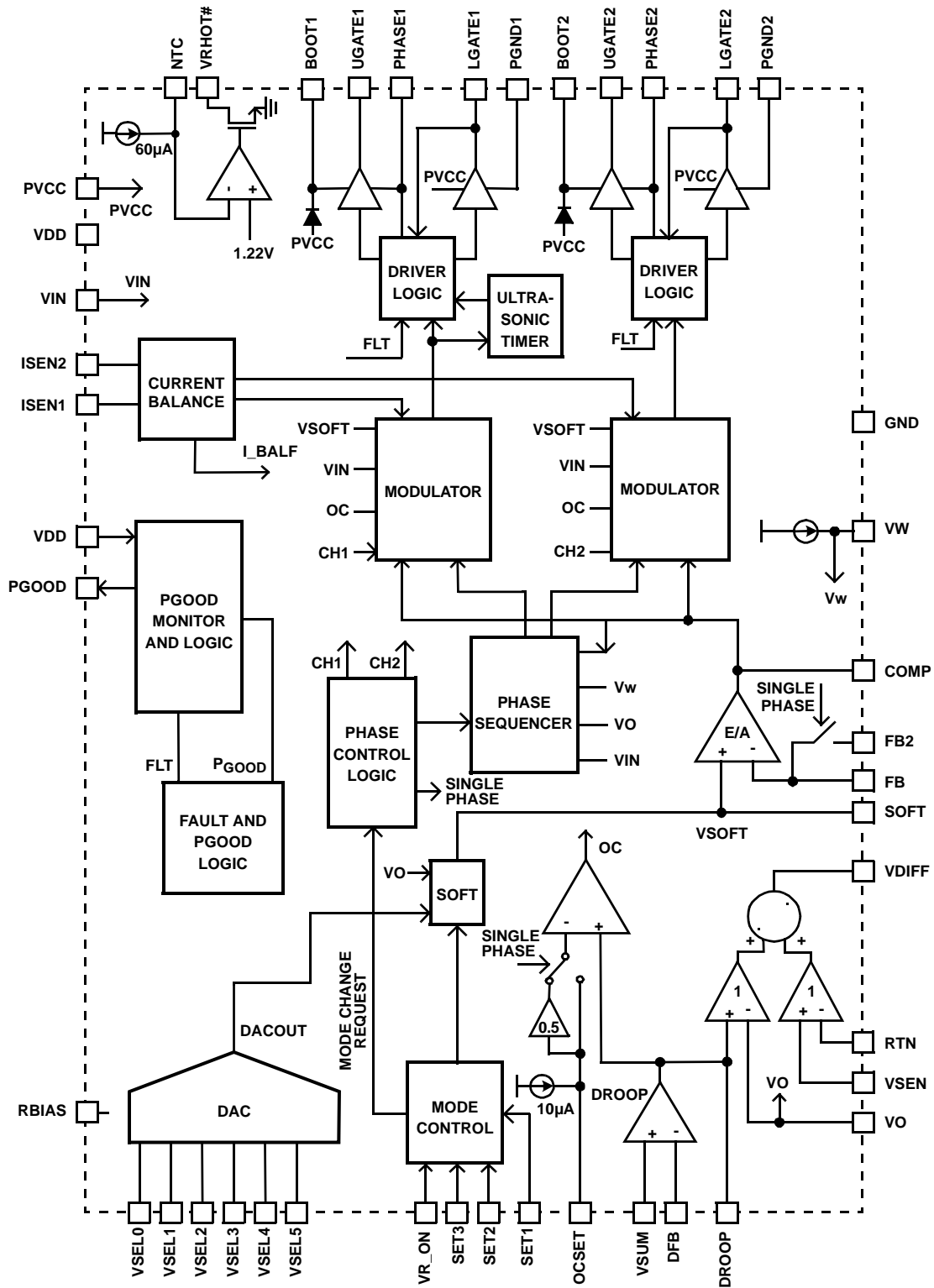
FIGURE 1. SIMPLIFIED FUNCTIONAL BLOCK DIAGRAM OF ISL9502

Typical Performance Curves 300kHz, DCR Sense, 2xIRF7821/2xIRF7832 Per Phase
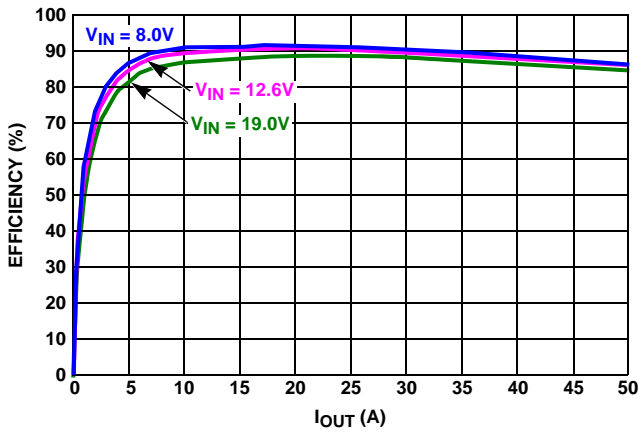
FIGURE 2. 2-PHASE CCM EFFICIENCY, VOUT = 1.15V
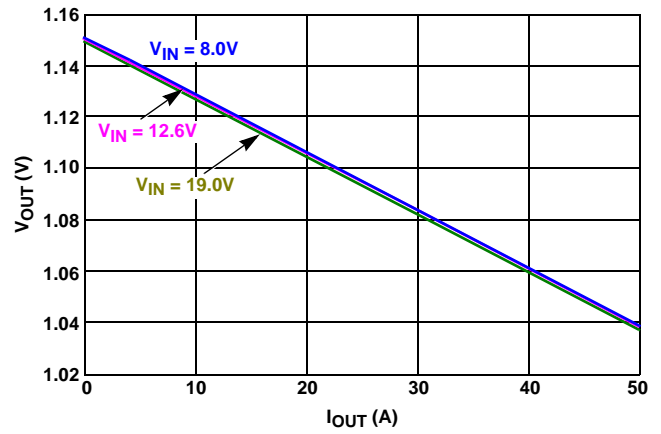
FIGURE 3. 2-PHASE CCM LOAD LINE, VOUT = 1.15V
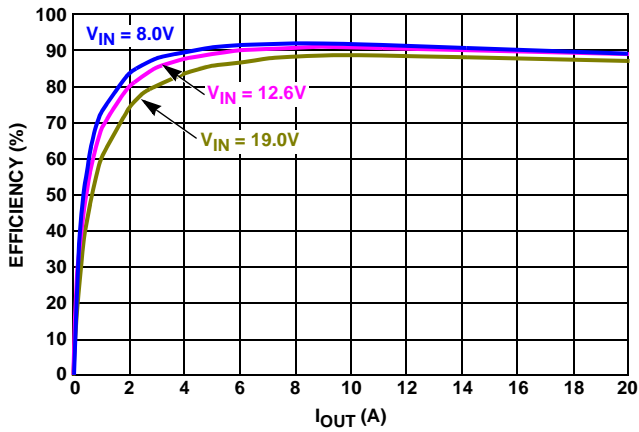
FIGURE 4. 1-PHASE CCM EFFICIENCY, VOUT = 1.15V
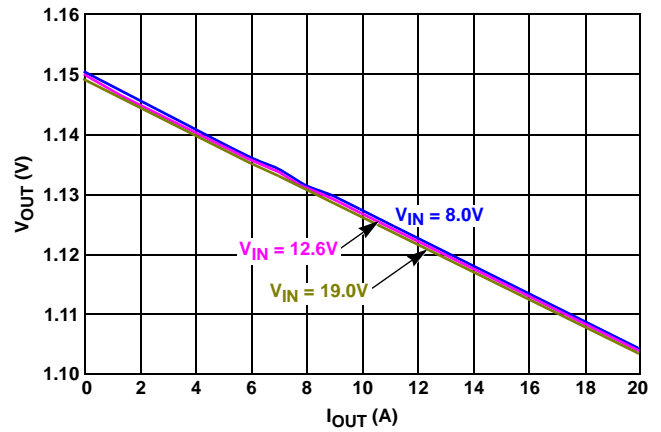
FIGURE 5. 1-PHASE CCM LOAD LINE, VOUT = 1.15V
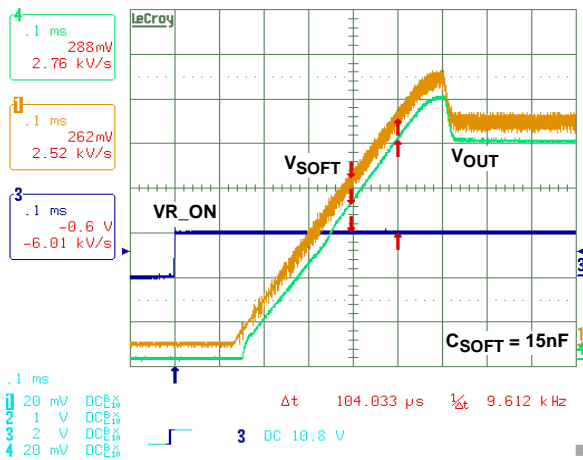
Typical Performance Curves

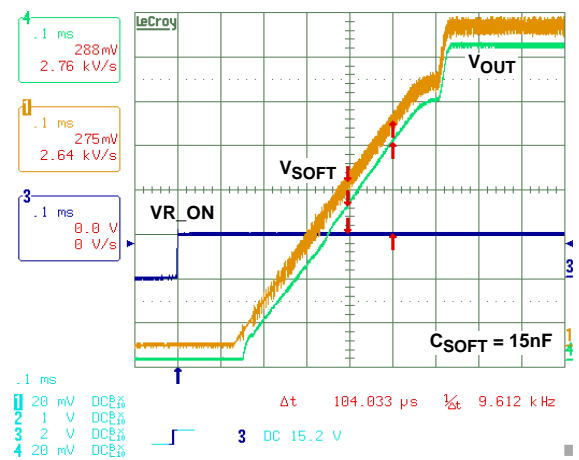FIGURE 6. SOFT-START WAVEFORM SHOWING SLEW RATE
OF 2.5mV/µs AT VSEL = 1V, I_{LOAD} = 10A

FIGURE 7. SOFT-START WAVEFORM SHOWING SLEW RATE
OF 2.5mV/µs AT VSEL = 1.4375V, I_{LOAD} = 10A

Typical Performance Curves (Continued)
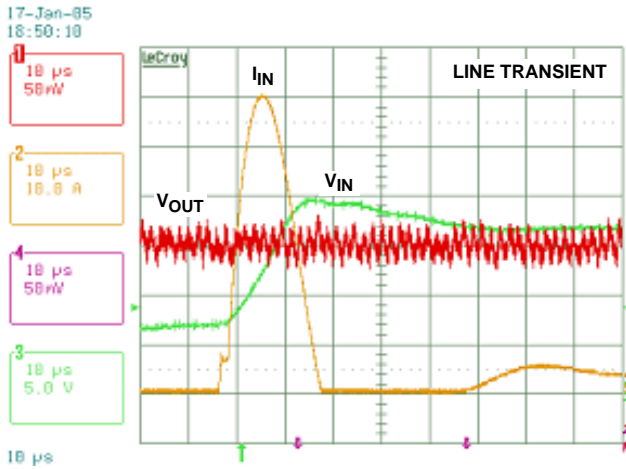
FIGURE 8. 8V-20V INPUT LINE TRANSIENT RESPONSE, C$_{IN}$ = 240µF
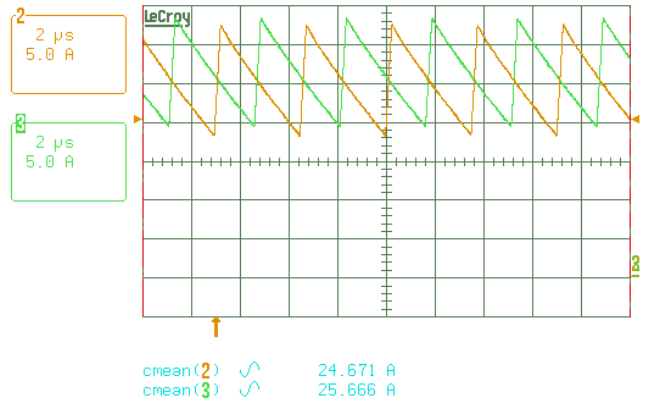
FIGURE 9. 2 PHASE CURRENT BALANCE, FULL LOAD = 50A
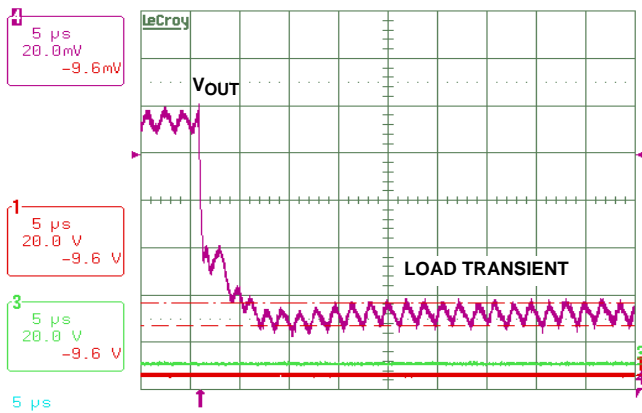
FIGURE 10. LOAD STEP-UP RESPONSE, 35A LOAD STEP @ 200A/µs, 2 PHASE CCM
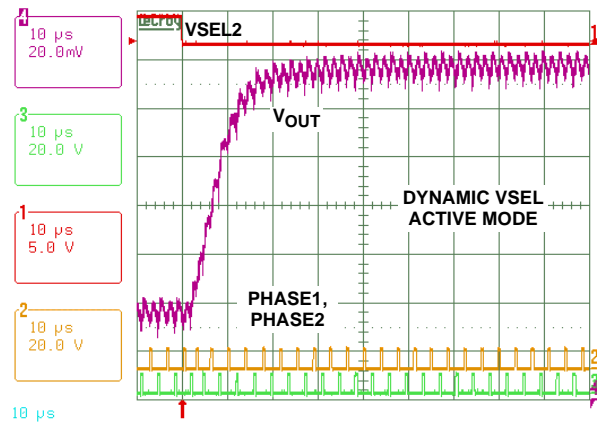
FIGURE 11. VSEL2 CHANGE OF FROM 1.0V TO 1.1V AT SET1 = 0, SET2 = 1, SET3 = 1
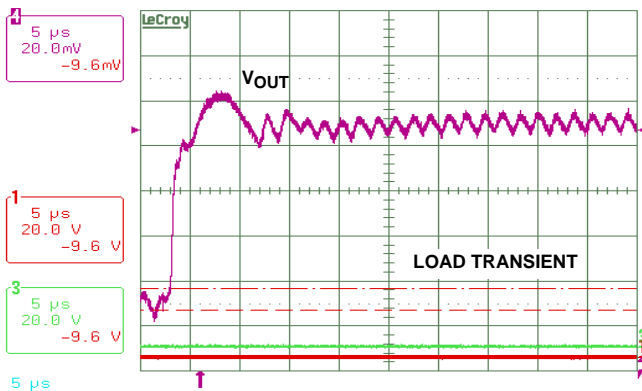
FIGURE 12. LOAD DUMP RESPONSE, 35A LOAD STEP @ 200A/µs, 2 PHASE CCM
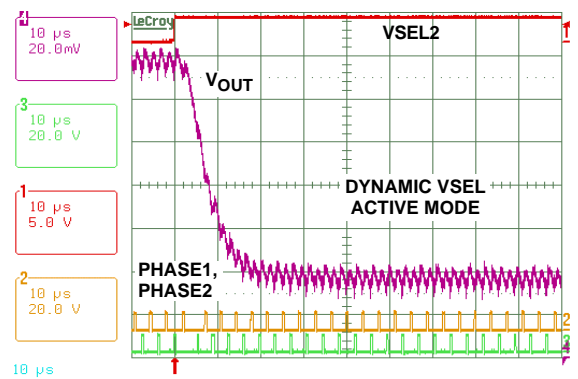
FIGURE 13. VSEL2 CHANGE FROM 1.1V TO 1V AT SET1 = 0, SET2 = 1, SET3 = 1

Typical Performance Curves (Continued)
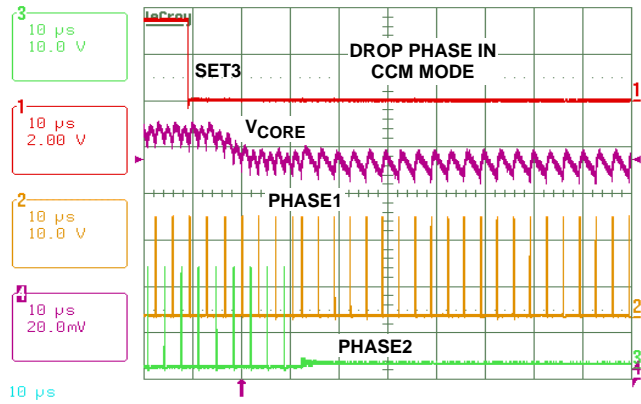
FIGURE 14. 2-PHASE CCM TO 1-PHASE CCM, AT SET1 = 0, SET2 = 1, I$_{LOAD}$ = 10A
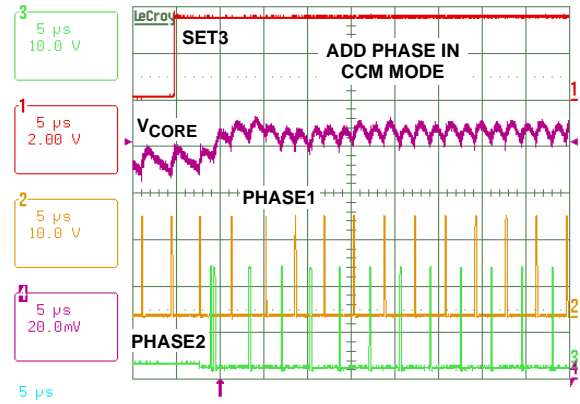
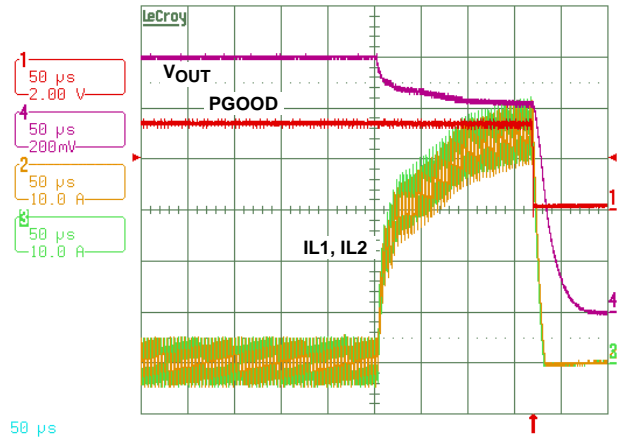FIGURE 15. 1-PHASE CCM TO 2-PHASE CCM, AT SET1 = 0, SET2 = 1

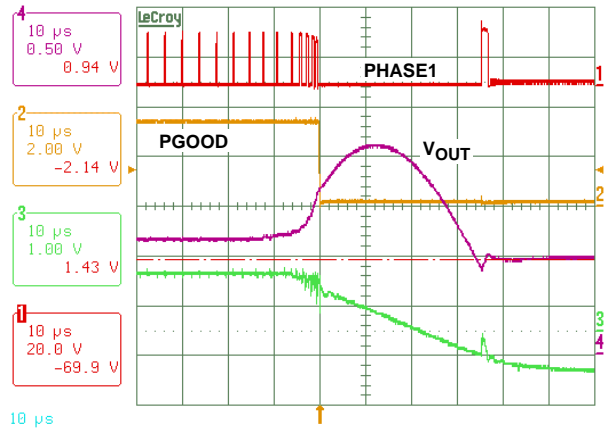FIGURE 16. OVERCURRENT PROTECTION

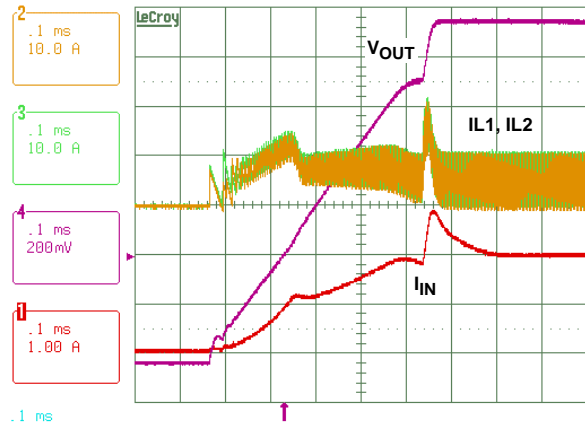FIGURE 17. 1.7V OVERVOLTAGE PROTECTION SHOWS OUTPUT VOLTAGE PULLED LOW TO 0.9V AND PWM THREE-STATE

FIGURE 18. INRUSH CURRENT AT START-UP, V$_{IN}$ = 8V, VOUT = 1.450V, I$_{LOAD}$ = 10A

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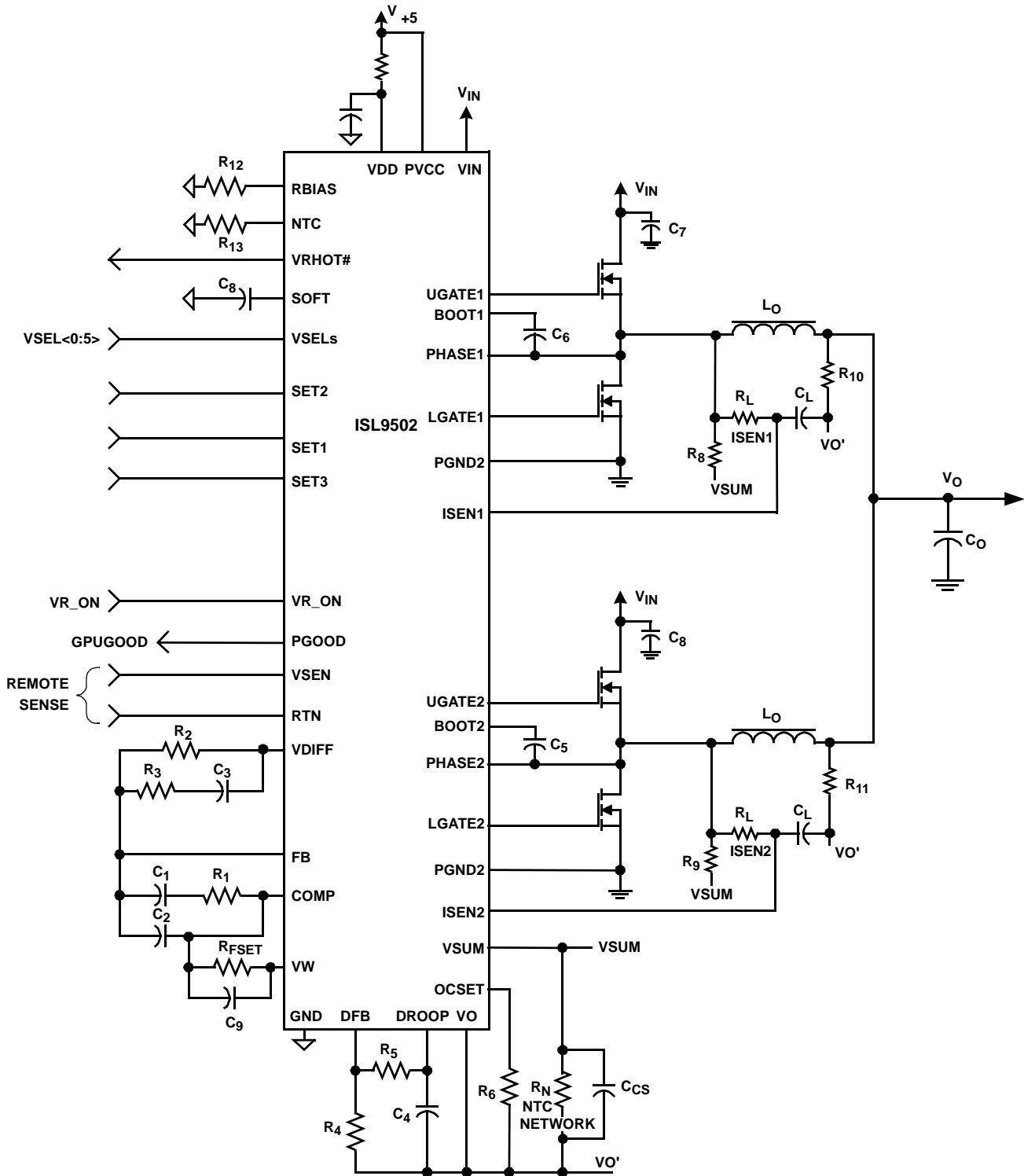## *Simplified Application Circuit for DCR Current Sensing*

FIGURE 19. ISL9502 BASED TWO-PHASE BUCK CONVERTER WITH INDUCTOR DCR CURRENT SENSING

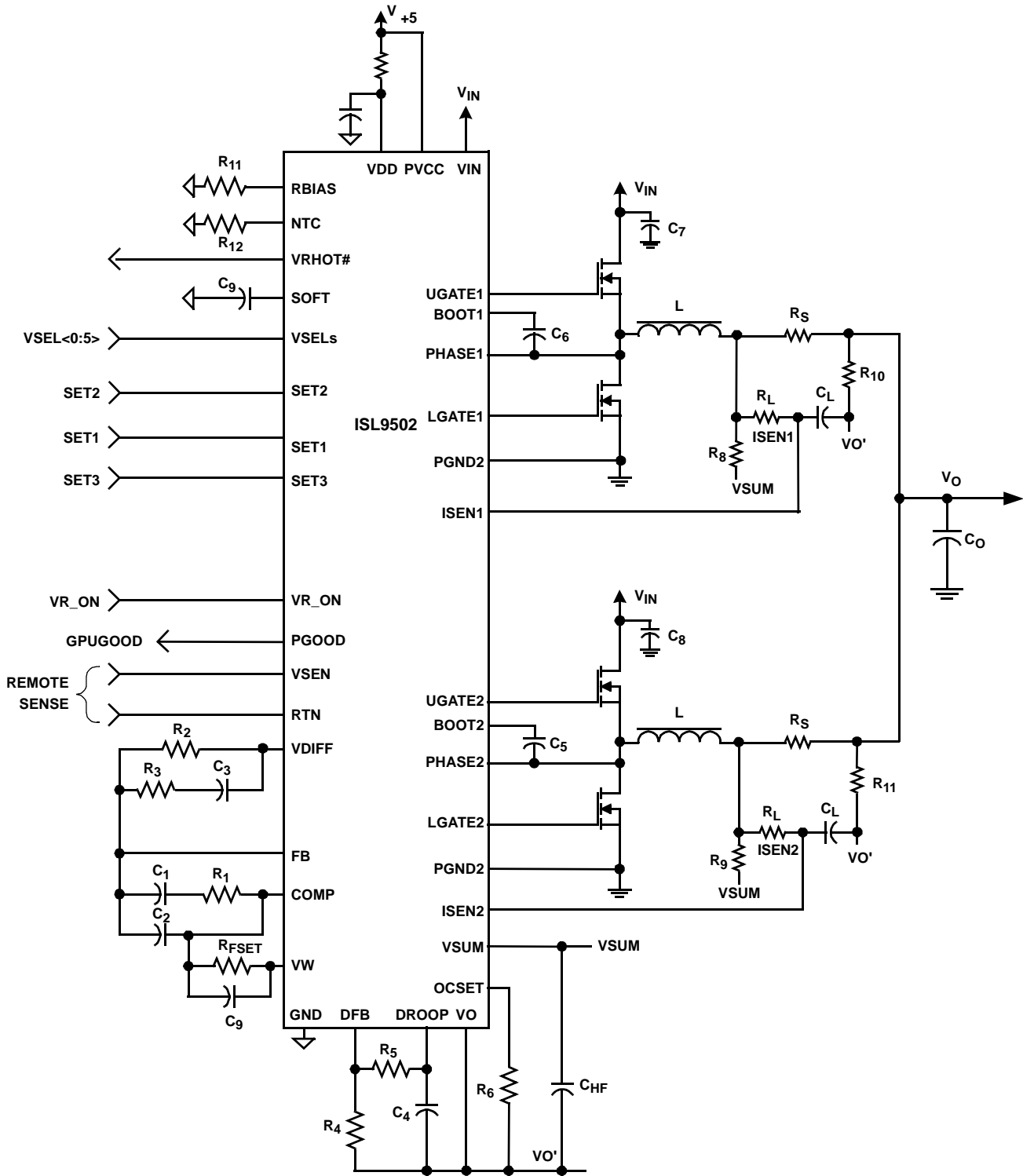## Simplified Application Circuit for Resistive Current Sensing

FIGURE 20. ISL9502 BASED TWO-PHASE BUCK CONVERTER WITH RESISTIVE CURRENT SENSING

Theory of Operation

The ISL9502 is a two-phase regulator including embedded gate drivers for reduced system cost and board area. The regulator provides optimum steady-state and transient performance for GPU applications up to 60A. System efficiency is enhanced by idling a phase at low-current and implementing DCM-mode operation.

The heart of the ISL9502 is the patented R3 (Robust Ripple Regulator®) modulator. The R3® modulator combines the best features of fixed frequency PWM and hysteretic PWM while eliminating many of their shortcomings. The ISL9502 modulator internally synthesizes an analog of the inductor ripple current and uses hysteretic comparators on those signals to establish PWM pulse widths. Operating on these large-amplitude, noise-free synthesized signals allows the ISL9502 to achieve lower output ripple and lower phase jitter than either conventional hysteretic or fixed frequency PWM controllers. Unlike conventional hysteretic converters, the ISL9502 has an error amplifier that allows the controller to maintain a 0.5% voltage regulation accuracy throughout the VSEL range from 0.7V to 1.5V.

The hysteresis window voltage is relative to the error amplifier output such that load current transients results in increased switching frequency, which gives the R3 regulator a faster response than conventional fixed frequency PWM controllers. Transient load current is inherently shared between active phases due to the use of a common hysteretic window voltage. Individual average phase voltages are monitored and controlled to equally share the static current among the active phases.

Start-Up Timing

With the controller's +5V VDD voltage above the POR threshold, the start-up sequence begins when VR_ON exceeds the 3.3V logic HIGH threshold. Approximately 100μs later, SOFT and VOUT begin ramping to the boot voltage of 1.2V. At startup, the regulator always operates in a 2-phase CCM mode, regardless of control signal assertion levels. During this internal, the SOFT cap is charged by 40μA current source. If the SOFT capacitor is selected to be 20nF, the SOFT ramp will be at 2mV/s for a soft-start time of 600s. Approximately 7ms later, PGOOD is asserted HIGH. The entire soft-start event is illustrated in Figure 21.

The ISL9502 is designed to always start up in 2-phase mode, then switch to the desired state as dictated by the states of the pins in Table 2. If a 1-phase design is implemented, the second phase will try to switch during start-up even though it is not connected to the system. This will not affect the start-up performance. After soft-start is complete, phase 2 will shut down and the controller will run continuously in 1-phase mode.
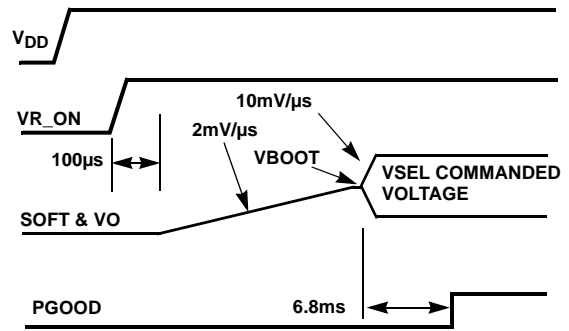

FIGURE 21. SOFT-START WAVEFORMS USING A 20nF SOFT CAPACITOR

Static Operation

After the start sequence, the output voltage will be regulated to the value set by the VSEL inputs per Table 1. The ISL9502 will control the no-load output voltage to an accuracy of ±0.5% over the range of 0.75V to 1.5V. The input of VSELs has to be actively pulled to logic high or logic low. Floating VSEL pins will leave logic-level vulnerable to noise-coupling.

TABLE 1. VSEL TABLE

VSEL<5:0>	VOUT	VSEL<5:0>	VOUT
000000	1.500	010101	0.975
000001	1.475	010110	0.950
000010	1.450	010111	0.925
000011	1.425	011000	0.900
000100	1.400	011001	0.875
000101	1.375	011010	0.850
000110	1.350	011011	0.825
000111	1.325	011100	0.800
001000	1.300	011101	0.775
001001	1.275	011110	0.750
001010	1.250	011111	0.725
001011	1.225	100000	0.700
001100	1.200	100001	0.675
001101	1.175	100010	0.650
001110	1.150	100011	0.625
001111	1.125	100100	0.600
010000	1.100	100101	0.575
010001	1.075	100110	0.550
010010	1.050	100111	0.525
010011	1.025	101000	0.500
010100	1.000		

A fully-differential amplifier implements core voltage sensing for precise voltage control at the remote-sense point. The inputs to the amplifier are the VSEN and RTN pins.

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As the load current increases from zero, the output voltage will droop from the VSEL table value by an amount proportional to current to achieve active voltage positioning. The ISL9502 provides for current to be measured using either resistors in series with the channel inductors as shown in the application circuit of Figure 2 or using the intrinsic series resistance of the inductors as shown in the application circuit of Figure 3. In both cases signals representing the inductor currents are summed at VSUM, which is the non-inverting input to the DROOP amplifier shown in the block diagram of Figure 1. The voltage at the DROOP pin minus the output voltage, VO´, is a high-bandwidth analog of the total inductor current. This voltage is used as an input to a differential amplifier to achieve active voltage positioning. This is also the input to the over-current protection circuit.

When using inductor DCR current sensing, a single NTC element is used to compensate the positive temperature coefficient of the copper winding, thus maintaining active voltage positioning.

In addition to monitoring the total current (used for DROOP and over-current protection), the individual channel average currents are monitored and used for balancing the load between channels. The IBAL circuit will adjust the channel pulse-widths up or down relative to the other channel to cause the voltages presented at the ISEN pins to be equal.

The ISL9502 controller can be configured for two-channel operation, with the channels operating 180° apart. The channel PWM frequency is determined by the value of R_{FSET} connected to pin VW as shown in Figure 2 and Figure 3. Input and output ripple frequencies will be the channel PWM frequency multiplied by the number of active channels.

High Efficiency Operation Mode

The ISL9502 has several operating modes to optimize efficiency. These operating modes are established by the control signal inputs SET1, SET2, and SET3 as shown in Table 2. At high current levels, the system can operate with both phases fully active, responding rapidly to transients and deliver the maximum power to the load. At reduced load current levels, one of the phases can be idled. This configuration will minimize switching losses, while still maintaining transient response capability. At the lowest current levels, the controller can be configured to operate in single-phase DCM mode, thus achieving the highest possible efficiency. In this mode of operation, the lower FET will be configured to automatically detect and prevent discharge current flowing from the output capacitor through the inductors, and the switching frequency will be proportionately reduced, thus greatly reducing both conduction and switching losses.

Smooth mode transitions are facilitated by the R3 Technology™, which correctly maintains the internally synthesized ripple currents throughout mode transitions. The controller is thus able to deliver the appropriate current to the load throughout mode transitions. The controller contains embedded mode-transition algorithms which robustly maintain voltage-regulation for all control signal input sequences and durations.

Timing of the mode transitions of ISL9502 has been carefully designed to work in concert with VSEL changes to minimize any perturbations to the output voltage. For example, transitions into single-phase mode will be delayed until any VSEL induced voltage ramp is complete to allow the associated output capacitor charging current to be shared by both inductor paths. While in single-phase automatic-DCM mode, VSEL changes will initiate an immediate return to two-phase CCM mode. This ensures that both inductor paths share the output capacitor charging current and are fully active for the subsequent load current increases.

The controller contains internal counters which prevent spurious control signal glitches from resulting in unwanted mode transitions. Control signals of less than two switching periods do not result in phase-idling. Signals of less than 7 switching periods do not result in implementation of DCM mode.

TABLE 2. CONTROL SIGNAL TRUTH TABLES FOR OPERATION MODES OF ISL9502

SET1	SET2	SET3	PHASE OPERATION MODES
0	0	0	1-phase CCM
0	0	1	2-phase CCM
0	1	0	1-phase CCM
0	1	1	2-phase CCM
1	0	0	1-phase diode emulation
1	0	1	1-phase diode emulation
1	1	0	1-phase CCM
1	1	1	2-phase CCM

ISL9502

While transitioning to single-phase operation, the controller smoothly transitions current from the idling-phase to the active-phase, and detects the idling-phase zero-current condition. During transitions into DCM or CCM mode, the timing is carefully adjusted to eliminate output voltage excursions. When a phase is added, the current balance between phases is quickly restored.

While SET3 is high, both phases are switching. If SET3 is asserted low and either SET2 or SET1 are not asserted, the controller will transition to CCM operation with only phase 1 switching, and both FET's of phase 2 will be off. The controller will thus eliminate switching losses associated with the unneeded channel.

When SET3, SET2, and SET1 are all asserted, the controller will transition to single-phase DCM mode. In this mode, both FET's associated with phase 2 will be off, and the ISL9502 will turn-off the lower FET of channel 1 whenever the channel 1 current decays to zero. As load is further reduced, the phase 1 channel switching frequency will decrease, thus maintaining high efficiency.

Protection

The ISL9502 provides overcurrent, overvoltage, under-voltage protection and over-temperature protection as shown in Table 3.

Overcurrent protection is tied to the voltage droop which is determined by the resistors selected as described in the "Component Selection and Application" section. Once a load-line is selected, large or small, a corresponding overcurrent set resistor can be chosen. An overcurrent fault will occur when the load current exceeds the overcurrent

setpoint voltage while the regulator is in a 2-phase mode. While the regulator is in a 1-phase mode of operation, the overcurrent setpoint is automatically reduced by half. For overcurrents less than twice the OCSET level, the over-load condition must exist for 120µs in order to trip the OC fault latch. This is shown in Figure 16.

For over-loads exceeding twice the set level, the PWM outputs will immediately shut off and PGOOD will go low to maximize protection due to hard shorts.

In addition, excessive phase imbalance, due to gate driver failure for example, will be detected in two-phase operation and the controller will be shut-down one millisecond after the imbalance is detected. A phase current mismatch is detected when the voltage measured between the ISEN pins is greater than 7.5mV.

Undervoltage protection is independent of the overcurrent limit. If the output voltage is less than VSEL - 300mV for one millisecond, a fault will be detected and the IC will latch off. The PWM outputs will turn off and PGOOD will go low. Note that most practical core regulators will have the overcurrent set to trip before the -300mV undervoltage limit.

There are two levels of overvoltage protection and response. For output voltage exceeding the set value by +200mV for one millisecond, a fault is declared. All of the above faults have the same action taken; PGOOD is latched low and the upper and lower power FETs are turned off so that inductor current will decay through the FET body diodes. This condition can be reset by bringing VR_ON low or by bringing VDD below 4V. When these inputs are returned to their high operating levels, a soft-start will occur.

TABLE 3. FAULT-PROTECTION SUMMARY OF ISL9502

	FAULT DURATION PRIOR TO PROTECTION	PROTECTION ACTIONS	FAULT RESET
Overcurrent fault	120µs	PWM1, PWM2 three-state, PGOOD latched low	VR_ON toggle or VDD toggle
Severe-Overcurrent fault	<2µs	PWM1, PWM2 three-state, PGOOD latched low	VR_ON toggle or VDD toggle
Overvoltage fault (1.7V)	Immediately	Low-side FET on until Vcore <0.85V, then PWM three-state, PGOOD latched low (OV-1.7V always)	VDD toggle
Overvoltage fault (+200mV)	1ms	PWM1, PWM2 three-state, PGOOD latched low	VR_ON toggle or VDD toggle
Undervoltage fault (-300mV)	1ms	PWM1, PWM2 three-state, PGOOD latched low	VR_ON toggle or VDD toggle
Unbalance fault (7.5mV)	1ms	PWM1, PWM2 three-state, PGOOD latched low	VR_ON toggle or VDD toggle
Over-temperature fault (NTC <1.18V)	Immediately	VRHOT# goes low	N/A

Refer to Figure 17, the second level of overvoltage protection behaves differently. If the output exceeds 1.7V, an OV fault is immediately declared, PGOOD is latched low and the low-side FETs are turned on. The low-side FETs will remain on until the output voltage is pulled down below about 0.85V at which time all FETs are turned off. If the output again rises above 1.7V, the protection process is repeated. This offers the maximum amount of protection against a shorted high-side FET while preventing output ringing below ground. The 1.7V OV cannot be reset with VR_ON, but rather requires that VDD power be recycled. The 1.7V OV detector is active at all times that the controller is enabled, including after one of the other faults occurs so that the processor is protected against high-side FET leakage while the FETs are commanded off.

The ISL9502 has a thermal throttling feature. If the voltage on the NTC pin goes below the 1.18V over-temperature threshold, the VRHOT# pin is pulled low indicating the need for thermal throttling to the system oversight processor. No other action is taken within the ISL9502 in response to NTC pin voltage.

Component Selection and Application

Soft-Start and Mode Change Slew Rates

The ISL9502 uses 2 slew rates for various modes of operation. The first is a slow slew rate, used to reduce inrush current during start-up. It can also be used to reduce audible noise when entering or exiting the different modes of operation outlined in Table 2. The assertion of SET1 HIGH produces a faster slew rate than when it is asserted LOW. Faster slew rates to exit DCM mode enhances system performance by achieving full synchronous regulation more quickly. Note that the SOFT cap current is bidirectional. The current is flowing into the SOFT capacitor when the output voltage is commanded to rise, and out of the SOFT capacitor when the output voltage is commanded to fall.

The two slew rates are determined by commanding one of two current sources onto the SOFT pin. As can be seen in Figure 22, the SOFT pin has a capacitance to ground. Also, the SOFT pin is the input to the error amplifier and is, therefore, the commanded system voltage. Depending on the state of the system, one of the two currents shown in Figure 22 will be used to charge or discharge this capacitor, thereby controlling the slew rate of the commanded voltage. These currents can be found under the SOFT-START CURRENT section of the Electrical Specification Table.
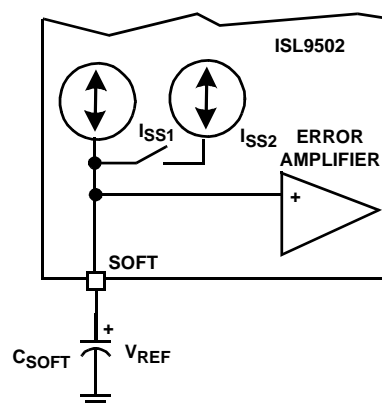

FIGURE 22. SOFT PIN CURRENT SOURCES FOR FAST AND SLOW SLEW RATES

The first current, labelled I_{SS1}, is given in the Specification Table as 41µA. This current is used during soft-start. The second current, I_{SS2} sums with I_{SS1} to get the larger of the two currents, labelled I_{ST} in the Electrical Specification Table. This total current is typically 200µA with a minimum of 175µA.

Equation 1 dictates how to program the desired fast slew rate of VSEL and mode transitions, where RATE represents the desired dV/dt for the application.

$$C_{SOFT} = \frac{I_{ST}}{RATE} \qquad (EQ. 1)$$

Using a SLEWRATE of 10mV/µs, and the typical I_{ST} value given in the Electrical Specification Table, C_{SOFT} is

$$C_{SOFT} = 200\mu A/(10mV/1\mu s) \qquad (EQ. 2)$$

A choice of 0.015µF would guarantee a RATE of 10mV/µs is met for minimum I_{ST} value, given in the Electrical Specification Table. With this C_{SOFT} selection, the slower dV/dt, from VR_ON assertion to VBOOT voltage (1.2V), is given by the following equation:

$$\frac{dV}{dt} = \frac{I_{SS}}{C_{SOFT}} = \frac{41\mu A}{0.015\mu F} = 2.8mV/\mu s \qquad (EQ. 3)$$

Selecting RBIAS

To properly bias the ISL9502, a reference current is established by placing a 147kΩ, 1% tolerance resistor from the RBIAS pin to ground. This will provide a highly accurate, 10µA current source from which OCSET reference current can be derived.

Care should be taken in layout that the resistor is placed very close to the RBIAS pin and that a good quality signal ground is connected to the opposite side of the RBIAS resistor. Do not connect any other components to this pin as this would negatively impact performance. Capacitance on this pin would create instabilities and should be avoided.

Static Mode of Operation - Remote Differential Sensing

Remote differential sensing is the ability of the controller to regulate the core output voltage at a remotely sensed point. This allows the voltage regulator to compensate for various resistive drops in the power path and ensure that the voltage seen at the GPU is the correct level independent of load current.

The VSEN and RTN pins of the ISL9502 are connected to the desired Kelvin sense points at the processor. This allows the voltage regulator to tightly control the processor voltage at the point of load, independent of layout inconsistencies and voltage drops. This Kelvin sense technique provides for extremely tight load line regulation. Some GPUs may provide two dedicated pins that report the core voltage on chip. These can be used to further increase accuracy by eliminating impedances found in the GPU socket.

These traces should be laid out as noise sensitive traces. For optimum load line regulation performance, the traces connecting these two pins to the Kelvin sense leads at the processor must be laid out away from rapidly rising voltage nodes, (switching nodes) and other noisy traces. To achieve optimum performance, place common mode and differential mode RC filters to analog ground on VSEN and RTN as shown in Figure 23. The filter resistors should be 10Ω so that they do not interact with the 50kΩ input resistance of the differential amplifier. The filter resistor may be inserted between +VOUT_SENSE and VSEN pin. Another option is to place to the filter resistor between +VOUT_SENSE and VSEN pin and between -VOUT_SENSE and RTN pin. The

need for these RC filters depends on the actual board layout and noise environment.

If on chip Kelvin sensing is used, it is recommended to include two resistors to assure a closed-loop output connection if the GPU is not present. Figure 23 illustrates the use of R_{OPN1} and R_{OPN2} to make a local feedback connection to output capacitance. These resistors typically range from 20 to 100Ω.

Setting the Switching Frequency - FSET

The R^3 modulator scheme is not a fixed frequency PWM architecture. The switching frequency can increase during the application of a load to improve transient performance.

It also varies slightly due changes in input and output voltage and output current, but this variation is normally less than 10% in continuous conduction mode.

Refer to Figure 19, the resistor connected between the VW and COMP pins of the ISL9502 adjusts the switching window, and therefore adjusts the switching frequency. The R_{FSET} resistor that sets up the switching frequency of the converter operating in CCM can be determined using the following relationship, where R_{FSET} is in kΩ and the switching period is in μs. Place a 47pF capacitor in parallel with the frequency set resistor for better noise immunity. In discontinuous conduction mode (DCM), the ISL9502 runs in period stretching mode. The switching frequency is dependent on the load current level.

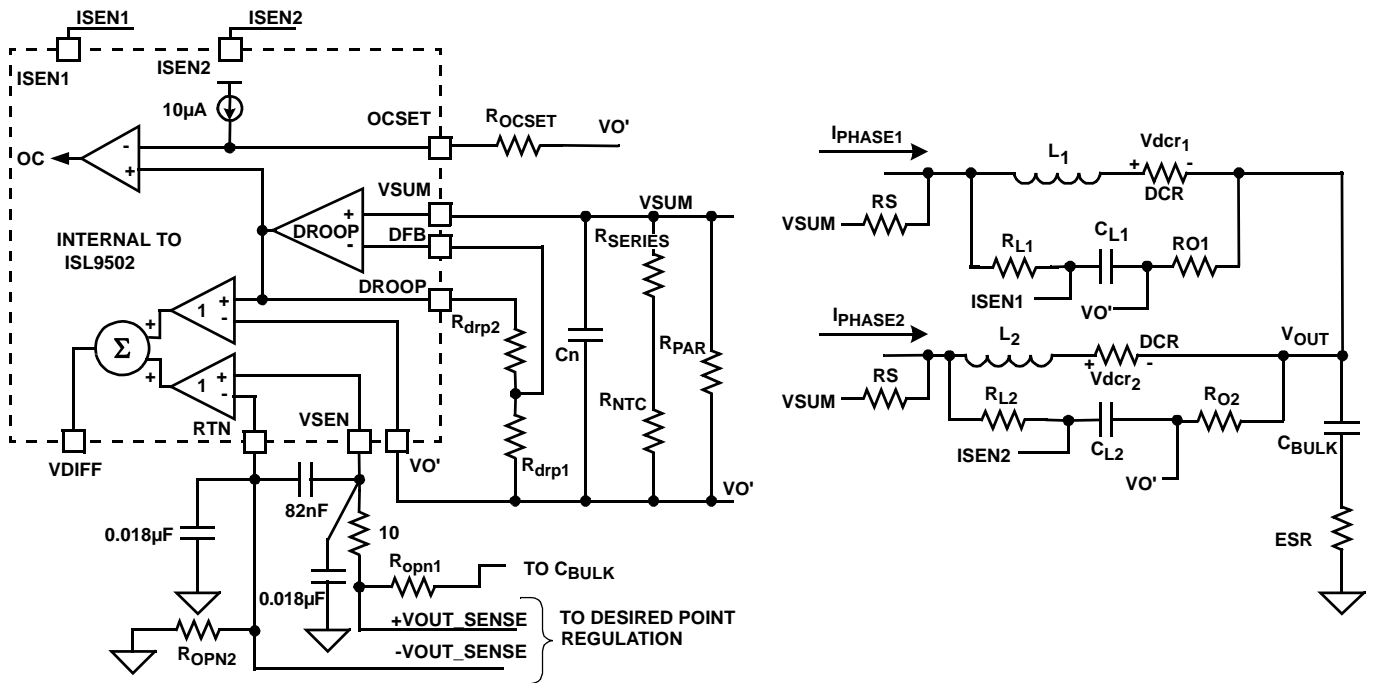$$R_{FSET}(k\Omega) \cong (period(\mu s) - 0.5) \bullet 1.56 \qquad (EQ. 4)$$

FIGURE 23. SIMPLIFIED SCHEMATIC FOR DROOP AND DIE SENSING WITH INDUCTOR DCR CURRENT SENSING

In general, the lighter the load, the slower the switching frequency. Therefore, the switching loss is much reduced for the light load operation, which is important for conserving the battery power in the portable application.

Voltage Regulator Thermal Throttling

The ISL9502 features a thermal monitor which senses the voltage change across an externally placed negative temperature coefficient (NTC) thermistor.

Proper selection and placement of the NTC thermistor allows for detection of a designated temperature rise by the system. Figure 24 shows the thermal throttling feature with hysteresis. At low temperature, SW1 is on and SW2 connects to the 1.18V side. The total current going into NTC pin is 60µA. The voltage on NTC pin is higher than threshold voltage of 1.18V and the comparator output is low. VRHOT# is pulling up high by the external resistor.
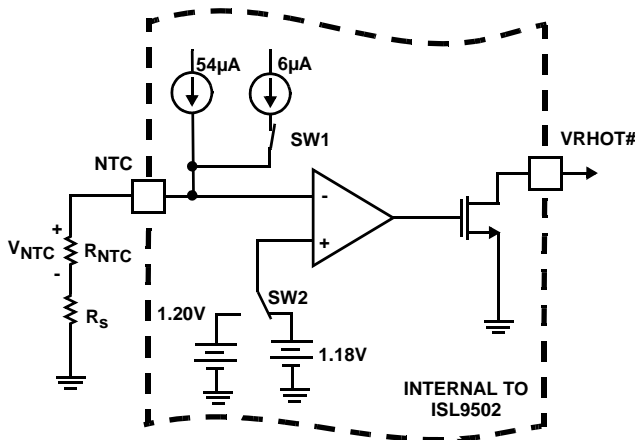

FIGURE 24. CIRCUITRY ASSOCIATED WITH THE THERMAL THROTTLING FEATURE IN ISL9502

When temperature increases, the NTC resistor value on NTC pin decreases. Thus, the voltage on NTC pin decreases to a level lower than 1.18V. The comparator output changes polarity and turns SW1 off and connects SW2 to 1.20V. This pulls VRHOT# low and sends the signal to start thermal throttle. There is a 6µA current reduction on NTC pin and 20mV voltage increase on threshold voltage of the comparator in this state. The VRHOT# signal can be used to change the GPU operation and decrease the power consumption. When the temperature goes down, the NTC thermistor voltage will eventually go up. The NTC pin voltage increases to 1.20V, the comparator output will then be able to flip back. Such a temperature hysteresis feature of VRHOT# is illustrated in Figure 25. T_1 represents the higher temperature point at which the VRHOT# goes from low to high due to the system temperature rise. T_2 represents the lower temperature point at which the VRHOT# goes high from low because the system temperature decreases to the normal level.
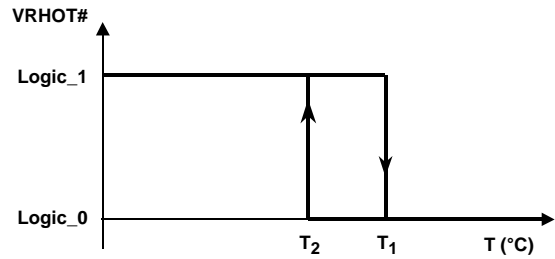

FIGURE 25. TEMPERATURE HYSTERESIS OF VRHOT#

Usually, the NTC thermistor's resistance can be approximated by the following formula:

$$R_{NTC}(T) = R_{NTCTo} \bullet e^{b \bullet \left(\frac{1}{T + 273} - \frac{1}{To + 273} \right)} \qquad \text{(EQ. 5)}$$

T is the temperature of the NTC thermistor and b is a parameter constant depending on the thermistor material. T_O is the reference temperature in which the approximation is derived. The most common temperature for T_O is 25°C. For example, there are commercial NTC thermistor products with b = 2750k, b = 2600k, b = 4500k or b = 4250k.

From the operation principle of the VRHOT# circuit explained, the NTC resistor satisfies the following equation group.

$$R_{NTC}(T_1) + R_S = \frac{1.18V}{60\mu A} = 19.67k\Omega \qquad \text{(EQ. 6)}$$

$$R_{NTC}(T_2) + R_S = \frac{1.2V}{54\mu A} = 22.22k\Omega \qquad \text{(EQ. 7)}$$

From Equation 6 and Equation 7, the following can be derived,

$$R_{NTC}(T_2) - R_{NTC}(T_1) = 2.55k\Omega \qquad \text{(EQ. 8)}$$

Using Equation 5 into Equation 8, the required nominal NTC resistor value can be obtained by:

$$R_{NTCTo} = \frac{2.55k\Omega \bullet e^{b \bullet \left(\frac{1}{T_o + 273} \right)}}{e^{b \bullet \left(\frac{1}{T_2 + 273} \right)} - e^{b \bullet \left(\frac{1}{T_1 + 273} \right)}} \qquad \text{(EQ. 9)}$$

For some cases, the constant b is not accurate enough to approximate the NTC resistor value, the manufacturer provides the resistor ratio information at different temperature. The nominal NTC resistor value may be expressed in another way as follows:

$$R_{NTCTo} = \frac{2.55k\Omega}{\overset{\Lambda}{R}_{NTC-T_2} - \overset{\Lambda}{R}_{NTC-T_1}} \qquad \text{(EQ. 10)}$$

where $\overset{\Lambda}{R}_{NTC-T}$ is the normalized NTC resistance to its nominal value. Most datasheet of the NTC thermistor gives the normalized resistor value based on its value at 25°C.

Once the NTC thermistor resistor is determined, the series resistor can be derived by:

$$R_S = \frac{1.18V}{60\mu A} - R_{NTC}(T1) = 19.67k\Omega - R_{NTC\_T_1} \qquad \text{(EQ. 11)}$$

Once R_{NTCT_0} and R_S is designed, the actual NTC resistance at T_2 and the actual T_2 temperature can be found in:

$$R_{NTC\_T_2} = 2.55k\Omega + R_{NTC\_T_1} \qquad \text{(EQ. 12)}$$

$$T_{2\_actual} = \frac{1}{\frac{1}{b}\ln\left(\frac{R_{NTC\_T_2}}{R_{NTCT_0}}\right) + 1/(273 + To)} - 273 \qquad \text{(EQ. 13)}$$

One example of using Equations 9, 10 and 11 to design a thermal throttling circuit with the temperature hysteresis 100°C to 105°C is illustrated as follows. Since T_1 = 105°C and T_2 = 100°C, if we use a Panasonic NTC with B = 4700, the Equation 9 gives the required NTC nominal resistance as

$$R_{NTC\_To} = 396k\Omega$$

In fact, the datasheet gives the resistor ratio value at 100°C to 105°C, which is 0.03956 and 0.03322 respectively. The b value 4700K in Panasonic datasheet only covers to 85°C. Therefore, using Equation 10 is more accurate for 100°C design, the required NTC nominal resistance at 25°C is 402kΩ. The closest NTC resistor value from manufacturer is 470kΩ. So the series resistance is given by Equation 11 as follows:

$$R_S = 19.67k\Omega - R_{NTC\_105°C} = 19.67k\Omega - 15.65k\Omega = 4.067k\Omega$$

Furthermore, the NTC resistance at T_2 is given by Equation 12.

$$R_{NTC\_T2} = 2.55k\Omega + R_{NTC\_T1} = 18.16k\Omega$$

From the NTC datasheet, it can be concluded that the actual temperature T_2 is about 97°C. If using the Equation 13, T_2 is calculated to be 97.7°C. Check the NTC datasheet to decide whether Equation 9 or Equation 10 can accurately represent the NTC resistor value at the designed temperature range.

Therefore, the NTC branch is designed to have a 470k NTC and 4.02k resistor in series. The part number of the NTC thermistor is ERTJ0EV474J. It is a 0402 package. The NTC thermistor should be placed in the spot which gives the best indication of the temperature of voltage regulator circuit. The actual hysteresis temperature is about 105°C and 97°C.

Static Mode of Operation - Static Droop Using DCR Sensing

As previously mentioned, the ISL9502 has an internal differential amplifier which provides for very accurate voltage regulation at the die of the processor. The load line regulation is also accurate for both two-phase and single-phase operation. The process of selecting the components for the appropriate load line droop is explained here.

For DCR sensing, the process of compensation for DCR resistance variation to achieve the desired load line droop has several steps and is somewhat iterative.

The two-phase solution using DCR sensing is shown in Figure 23. There are two resistors connecting to the terminals of inductor of each phase. These are labelled RS and RO. These resistors are used to obtain the DC voltage drop across each inductor. Each inductor will have a certain level of DC current flowing through it, and this current when multiplied by the DCR of the inductor creates a small DC voltage drop across the inductor terminal. When this voltage is summed with the other channels DC voltages, the total DC load current can be derived.

RO is typically 1 to 10Ω. This resistor is used to tie the outputs of all channels together and thus create a summed average of the local CORE voltage output. RS is determined through an understanding of both the DC and transient load currents. This value will be covered in the next section. However, it is important to keep in mind that the output of each of these RS resistors are tied together to create the VSUM voltage node. With both the outputs of RO and RS tied together, the simplified model for the droop circuit can be derived. This is presented in Figure 26.

Figure 26 shows the simplified model of the droop circuitry. Essentially one resistor can replace the RO resistors of each phase and one RS resistor can replace the RS resistors of each phase. The total DCR drop due to load current can be replaced by a DC source, the value of which is given by:

$$V_{DCR\_EQU} = \frac{I_{OUT} \cdot DCR}{2} \qquad \text{(EQ. 14)}$$

For the convenience of analysis, the NTC network comprised of Rntc, Rseries and Rpar, given in Figure 23, is labelled as a single resistor Rn in Figure 26.

The first step in droop load line compensation is to adjust Rn, RO_{EQV} and RS_{EQV} such that sufficient droop voltage exists even at light loads between the VSUM and VO' nodes. As a rule of thumb we start with the voltage drop across the Rn network, VN, to be 0.5-0.8 times V_{DCR_EQU}. This ratio provides for a fairly reasonable amount of light load signal from which to arrive at droop.

The resultant NTC network resistor value is dependent on the temperature and given by

$$R_n(T) = \frac{(R_{series} + R_{ntc}) \cdot R_{par}}{R_{series} + R_{ntc} + R_{par}} \qquad \text{(EQ. 15)}$$

For simplicity, the gain of Vn to the V_{dcr_equ} is defined by G1, also dependent on the temperature of the NTC thermistor.
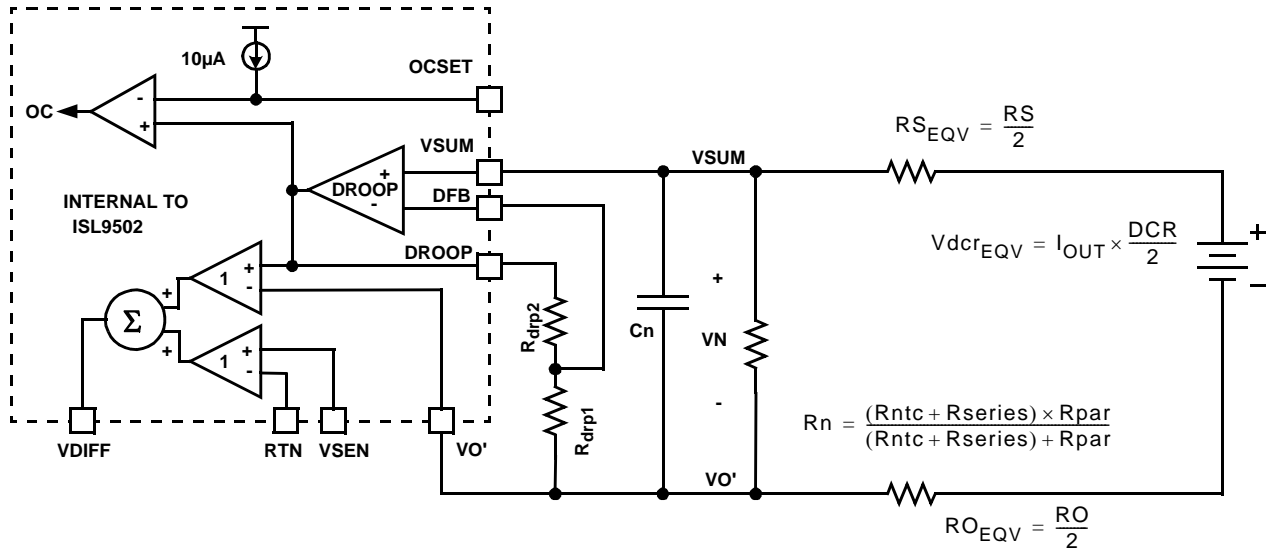
FIGURE 26. EQUIVALENT MODEL FOR DROOP AND DIE SENSING USING DCR SENSING

$$G_1(T) \overset{\Delta}{=} \frac{R_n(T)}{R_n(T) + RS_{EQV}} \qquad (EQ.\ 16)$$

$$DCR(T) = DCR_{25°C} \bullet (1 + 0.00393*(T\text{-}25)) \qquad (EQ.\ 17)$$

Therefore, the output of the droop amplifier divided by the total load current can be expressed as follows.

$$R_{droop} = G_1(T) \bullet \frac{DCR_{25}}{2} \bullet (1 + 0.00393*(T\text{-}25)) \bullet k_{droopamp} \qquad (EQ.\ 18)$$

where R_{droop} is the realized load line slope and 0.00393 is the temperature coefficient of the copper. To achieve the droop value independent from the temperature of the inductor, it is equivalently expressed by the following.

$$G_1(T) \bullet (1 + 0.00393*(T\text{-}25)) \cong G_{1target} \qquad (EQ.\ 19)$$

The non-inverting droop amplifier circuit has the gain $K_{droopamp}$ expressed as:

$$k_{droopamp} = 1 + \frac{R_{drp2}}{R_{drp1}}$$

$G_{1target}$ is the desired gain of Vn over $I_{OUT} \bullet DCR/2$. Therefore, the temperature characteristics of gain of Vn is described by:

$$G_1(T) = \frac{G_{1target}}{(1 + 0.00393*(T\text{-}25))} \qquad (EQ.\ 20)$$

For the $G_{1target}$ = 0.76, the Rntc = 10kΩ with b = 4300, Rseries = 2610kΩ, and Rpar = 11kΩ, RS_{EQV} = 1825Ω generates a desired G1, close to the feature specified in Equation 20. The actual G1 at 25°C is 0.763. For different G1 and NTC thermistor preference, the design file to generate the proper value of Rntc, Rseries, Rpar, and RS_{EQV} is provided by Intersil.

Then, the individual resistors from each phase to the VSUM node, labelled RS1 and RS2 in Figure 31, are then given by the following equation.

$$Rs = 2 \bullet RS_{EQV} \qquad (EQ.\ 21)$$

So, Rs = 3650Ω. Once we know the attenuation of the RS and RN network, we can then determine the droop amplifier gain required to achieve the load line. Setting R_{drp1} = 1k_1%, then R_{drp2} is can be found using equation

$$Rdrp2 = \left(\frac{2 \bullet R_{droop}}{DCR \bullet G1(25°C)} - 1\right) \bullet R_{drp1} \qquad (EQ.\ 22)$$

If a droop impedance (Rdroop) = 0.0018 (V/A) is used for example, DCR = 0.0008Ω typical for a 0.36µH inductor, R_{drp1} = 1kΩ and the attenuation gain (G1) = 0.77, R_{drp2} is then given by

$$Rdrp2 = \left(\frac{2 \bullet R_{droop}}{0.0008 \bullet 0.763} - 1\right) \bullet 1k\Omega \approx 4.90k\Omega$$

Note, we choose to ignore the RO resistors because they do not add significant error.

These designed values in Rn network are very sensitive to layout and coupling factor of the NTC to the inductor. As only one NTC is required in this application, this NTC should be placed as close to the Channel 1 inductor as possible and PCB traces sensing the inductor voltage should go directly to the inductor pads.

Once the board has been laid out, some adjustments may be required to adjust the full load droop voltage. This is fairly easy and can be accomplished by allowing the system to achieve thermal equilibrium at full load, and then adjusting R_{drp2} to obtain the appropriate load line slope.

To see whether the NTC has compensated the temperature change of the DCR, the user can apply full load current and wait for the thermal steady state and see how much the

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output voltage will deviate from the initial voltage reading. A good compensation can limit the drift to 2mV. If the output voltage is decreasing with temperature increase, that ratio between the NTC thermistor value and the rest of the resistor divider network has to be increased. The user should follow the evaluation board value and layout of NTC as much as possible to minimize engineering time.

The 1.8mV/A load line from the above example should be adjusted by R_{drp2} based on maximum current, not based on small current steps like 10A, as the droop gain might vary between each 10A steps. Basically, if the max current is 40A, the required droop voltage is 72mV. The user should have 40A load current on and look for 72mV droop. If the drop voltage is less than 72mV, for example, 68mV. The new value will be calculated by:

$$Rdrp2\_new = \frac{72mV}{68mV}(Rdrp1 + Rdrp2) - Rdrp1$$

For the best accuracy, the effective resistance on the DFB and VSUM pins should be identical so that the bias current of the droop amplifier does not cause an offset voltage. In the example above, the resistance on the DFB pin is R_{drp1} in parallel with Rdrop2, that is, 1K in parallel with 4.90K or 830Ω. The resistance on the VSUM pin is Rn in parallel with RS_{EQV} or 4.90K in parallel with 1.825K or 1392Ω. The mismatch in the effective resistances is 1392 - 830 = 562Ω. Do not let the mismatch get larger than 600Ω. To reduce the mismatch, multiply both R_{drp1} and R_{drp2} by the appropriate factor. The appropriate factor in the example is 1392/830 = 1.677.

Dynamic Mode of Operation - Dynamic Droop Using DCR Sensing

Droop is very important for load transient performance. If the system is not compensated correctly, the output voltage could sag excessively upon load application and potentially create a system failure. The output voltage could also take a long period of time to settle to its final value. This could be problematic if a load dump were to occur during this time. This situation would cause the output voltage to rise above the no load setpoint of the converter and could potentially damage the GPU.

The L/DCR time constant of the inductor must be matched to the Rn*Cn time constant as shown in the following equation:

$$\frac{L}{DCR} = \frac{R_n \bullet RS_{EQV}}{R_n + RS_{EQV}} \bullet C_n \qquad \text{(EQ. 23)}$$

Solving for Cn we now have the following equation:

$$C_n = \frac{\dfrac{L}{DCR}}{\dfrac{R_n \bullet RS_{EQV}}{R_n + RS_{EQV}}} \qquad \text{(EQ. 24)}$$

Note, RO was neglected. As long as the inductor time constant matches the Cn, Rn and Rs time constants as given above, the transient performance will be optimum. As in the static droop case, this process may require a slight adjustment to correct for layout inconsistencies. For the

example of L = 0.36µH with 0.8mΩ DCR, Cn is calculated below.

$$C_n = \frac{\dfrac{0.36\mu H}{0.0008}}{parallel(5.87K, 1.825K)} \approx 330nF \qquad \text{(EQ. 25)}$$

The value of this capacitor is selected to be 330nF. As the inductors tend to have 20% to 30% tolerances, this cap generally will be tuned on the board by examining the transient voltage. If the output voltage transient has an initial dip, lower than the voltage required by the load line, and slowly increases back to the steady state, the cap is too small and vice versa. It is better to have the cap value a little bigger to cover the tolerance of the inductor to prevent the output voltage from going lower than the spec. This cap needs to be a high grade cap like X7R with low tolerance. There is another consideration in order to achieve better time constant match mentioned above. The NPO/COG (class-I) capacitors have only 5% tolerance and a very good thermal characteristics. But those caps are only available in small capacitance values. In order to use such capacitors, the resistors and thermistors surrounding the droop voltage sensing and droop amplifier has to be resized up to 10X to reduce the capacitance by 10X. But attention has to be paid in balancing the impedance of droop amplifier in this case.

Dynamic Mode of Operation - Compensation Parameters

Considering the voltage regulator as a black box with a voltage source controlled by VSEL and a series impedance, in order to achieve the desired load line, the series impedance needs to match the load line impedance. The compensation design has to target the output impedance of the converter to be this value. There is a mathematical calculation file available to the user. The power stage parameters such as L and Cs are needed as the input to calculate the compensation component values. Attention has to be paid to the input resistor to the FB pin. Too high of a resistor will cause an error to the output voltage regulation because of bias current flowing in the FB pin. It is better to keep this resistor below 3K when using this file.

Static Mode of Operation - Current Balance Using DCR or Discrete Resistor Current Sensing

Current Balance is achieved in the ISL9502 through the matching of the voltages present on the ISEN pins. The ISL9502 adjusts the duty cycles of each phase to maintain equal potentials on the ISEN pins. RL and CL around each inductor, or around each discrete current resistor, are used to create a rather large time constant such that the ISEN voltages have minimal ripple voltage and represent the DC current flowing through each channel's inductor. For optimum performance, RL is chosen to be 10kΩ and CL is selected to be 0.22µF. When discrete resistor sensing is used, a capacitor most likely needs to be placed in parallel with RL to properly compensate the current balance circuit.

The ISL9502 uses RC filter to sense the average voltage on phase node and forces the average voltage on the phase node to be equal for current balance. Even though the ISL9502 forces the ISEN voltages to be almost equal, the inductor currents will not be exactly equal. Take DCR current sensing as example, two errors have to be added to find the total current imbalance. 1) Mismatch of DCR: If the DCR has a 5% tolerance, then the resistors could mismatch by 10% worst case. If each phase is carrying 20A then the phase currents mismatch by 20A*10% = 2A. 2) Mismatch of phase voltages/offset voltage of ISEN pins. The phase voltages are within 2mV of each other by current balance circuit. The error current that results is given by 2mV/DCR. If DCR = 1mΩ then the error is 2A.

In the above example, the two errors add to 4A. For the two phase DC/DC, the currents would be 22A in one phase and 18A in the other phase. In the above analysis, the current balance can be calculated with 2A/20A = 10%. This is the worst case calculation, for example, the actual tolerance of two 10% DCRs is 10%*sqrt(2) = 7%.

There are provisions to correct the current imbalance due to layout or to purposely divert current to certain phase for better thermal management. A customer can put a resistor in parallel with the current sensing capacitor on the phase of interest in order to purposely increase the current in that phase.

In the case the pc board trace resistance from the inductor to the microprocessor are not the same on two phases, the current will not be balanced. On the phase that have too much trace resistance a resistor can be added in parallel with the ISEN capacitor that will correct for the poor layout.

An estimate of the value of the resistor is:

Rtweak = Risen * Rdcr/(Rtrace-Rmin)

where Risen is the resistance from the phase node to the ISEN pin; usually 10kΩ. Rdcr is the DCR resistance of the inductor. Rtrace is the trace resistance from the inductor to the microprocessor on the phase that needs to be tweaked. It should be measured with a good microOhm meter. Rmin is the trace resistance from the inductor to the microprocessor on the phase with the least resistance.

For example, if the pc board trace on one phase is 0.5mΩ and on another trace is 0.3mΩ; and if the DCR is 1.2mΩ; then the tweaking resistor is
Rtweak = 10kΩ * 1.2/(0.5 - 0.3) = 60kΩ.

When choosing current sense resistor, not only the tolerance of the resistance is important, but also the TCR. And its combined tolerance at a wide temperature range should be calculated.

Droop Using Discrete Resistor Sensing - Static/Dynamic Mode of Operation

Figure 28 shows the equivalent circuit of a discrete current sense approach. Figure 20 shows a more detailed schematic of this approach. Droop is solved the same way as the DCR sensing approach with a few slight modifications.

First, there is no NTC required for thermal compensation, therefore, the Rn resistor network in the previous section is not required. Secondly, there is no time constant matching required, therefore, the Cn component is not matched to the L/DCR time constant. This component does indeed provide noise immunity and therefore is populated with a 39pF capacitor.

The RS values in the previous section, RS = 1.5k_1% are sufficient for this approach.

Now, the input to the droop amplifier is essentially the Vrsense voltage. This voltage is given by the following equation:

$$Vrsense_{EQV} = \frac{R_{sense}}{2} \bullet I_{OUT} \qquad (EQ. 26)$$

The gain of the droop amplifier, $K_{droopamp}$, must be adjusted for the ratio of the R_{sense} to droop impedance, Rdroop. We use the following equation:

$$K_{droopamp} = \frac{R_{droop}}{R_{sense}} \bullet 2 \qquad (EQ. 27)$$

Solving for the R_{drp2} value, Rdroop = 0.0018(V/A) from the previous NTC example, R_{sense} = 0.001Ω and R_{drp1} = 1kΩ, we obtain the following:

$$Rdrp2 = (K_{droopamp} - 1) \bullet R_{drp1} = 2.6k\Omega \qquad (EQ. 28)$$

These values are extremely sensitive to layout. Once the board has been laid out, some tweaking may be required to adjust the full load droop. This is fairly easy and can be accomplished by allowing the system to achieve thermal equilibrium at full load, and then adjusting R_{drp2} to obtain the desired droop value.

Fault Protection - Overcurrent Fault Setting

As previously described, the overcurrent protection of the ISL9502 is related to the droop voltage. Previously we have calculated that the droop voltage = ILoad * Rdroop, for an Rdroop that produces a load line slope of 0.0018 (V/A). Knowing this relationship, the overcurrent protection threshold can be set up as a voltage droop level. Knowing this voltage droop level, one can program in the appropriate drop across the Roc resistor. This voltage drop will be referred to as Voc. Once the droop voltage is greater than Voc, the PWM drives will turn off and PGOOD will go low.

The selection of Roc is given in equation. Assuming we desire an overcurrent trip level, Ioc, of 60A, and knowing that the load line slope, Rdroop is 0.0018 (V/A), we can then calculate for Roc as shown in equation.

$$R_{OC} = \frac{I_{OC} \bullet R_{droop}}{10\mu A} = \frac{60 \bullet 0.0018}{10 \bullet 10^{-6}} = 10.8k\Omega \qquad (EQ. 29)$$

Note, if the droop load line slope is not 0.0018 (V/A) in the application, the overcurrent setpoint will differ from predicted.
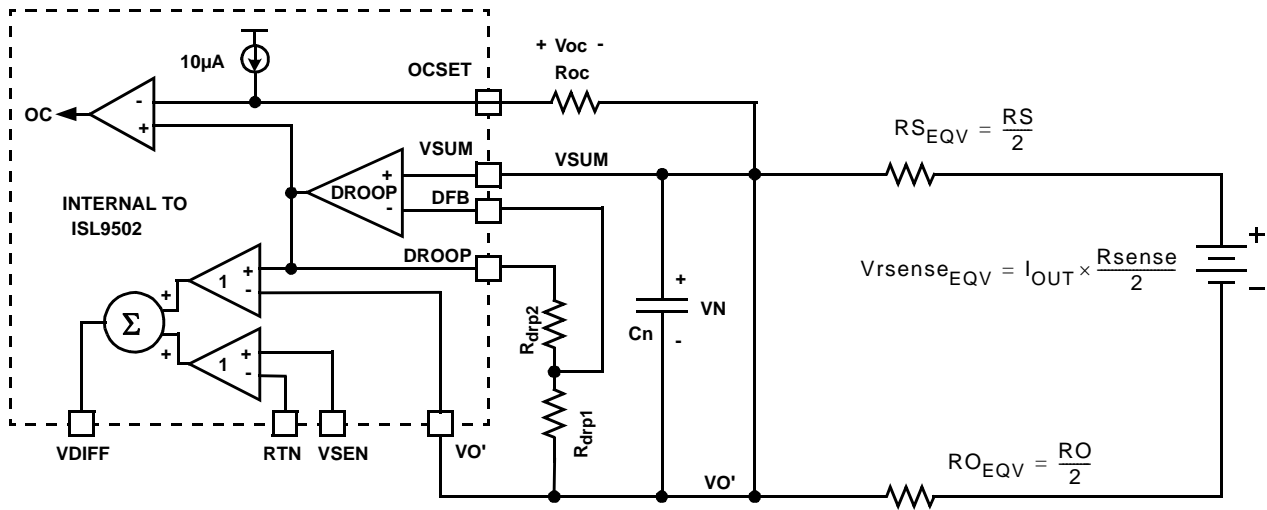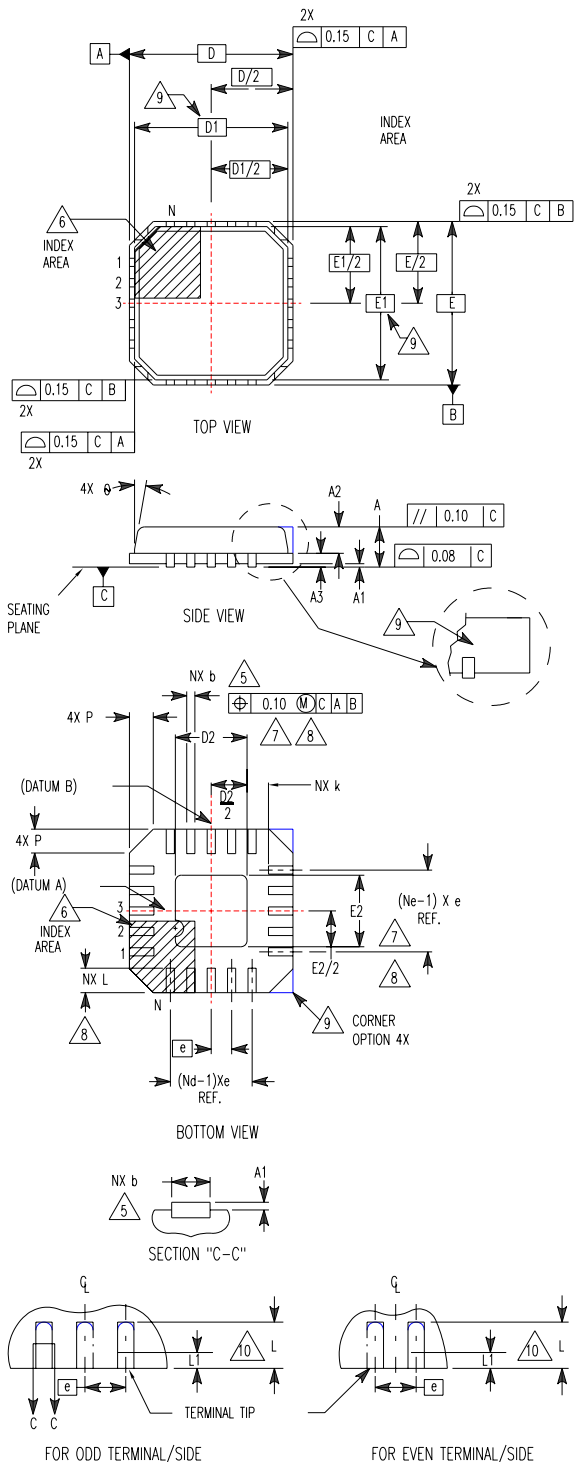

FIGURE 27. EQUIVALENT MODEL FOR DROOP AND DIE SENSING USING DISCRETE RESISTOR SENSING

Quad Flat No-Lead Plastic Package (QFN)
Micro Lead Frame Plastic Package (MLFP)

TOP VIEW

SIDE VIEW

BOTTOM VIEW

SECTION "C-C"

FOR ODD TERMINAL/SIDE

FOR EVEN TERMINAL/SIDE

L48.7x7
48 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE (COMPLIANT TO JEDEC MO-220VKKD-2 ISSUE C)

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	-	-	0.05	-
A2	-	-	1.00	9
A3	0.20 REF			9
b	0.18	0.23	0.30	5, 8
D	7.00 BSC			-
D1	6.75 BSC			9
D2	4.15	4.30	4.45	7, 8
E	7.00 BSC			-
E1	6.75 BSC			9
E2	4.15	4.30	4.45	7, 8
e	0.50 BSC			-
k	0.25	-	-	-
L	0.30	0.40	0.50	8
L1	-	-	0.15	10
N	48			2
Nd	12			3
Ne	12			3
P	-	-	0.60	9
θ	-	-	12	9

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NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.

2. N is the number of terminals.

3. Nd and Ne refer to the number of terminals on each D and E.

4. All dimensions are in millimeters. Angles are in degrees.

5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.

6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.

8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.

9. Features and dimensions A2, A3, D1, E1, P & θ are present when Anvil singulation method is used and not present for saw singulation.

10. Depending on the method of lead termination at the edge of the package, a maximum 0.15mm pull back (L1) maybe present. L minus L1 to be equal to or greater than 0.3mm.

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