

# TVS Diode

Transient Voltage Suppressor Diodes

## ESD300-B1-02LRH

Low Clamping & Low Capacitance ESD/Surge Protection Diode

ESD300-B1-02LRH

## Data Sheet

Revision 1.2, 2013-11-26  
Final

**Revision History: Revision 1.1, 2013-06-17**

Page or Item	Subjects (major changes since previous revision)
<b>Revision 1.2, 2013-11-26</b>	
4	Update of Figure 2-1)

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Last Trademarks Update 2010-10-26

# 1 Low Clamping & Low Capacitance ESD/Surge Protection Diode

## 1.1 Features

- Extremely high ESD and surge protection
  - IEC61000-4-2 (ESD):  $\pm 30$  kV (air/contact discharge)
  - IEC61000-4-5 (surge):  $\pm 18$  A (8/20  $\mu$ s)
- Low clamping voltage  $V_{CL} < 8$  V (8 kV contact)
- Maximum peak pulse power  $P_{PP} = 260$  W (8/20  $\mu$ s)
- Extremely low dynamic resistance:  $R_{DYN} = 0.23$   $\Omega$  typ.
- Supports applications with signal voltage 3.3 V max.
- Line capacitance:  $C_L = \text{typ. } 1.2$  pF
- Package TSLP-2-17 compatible to SOD882D leadless ultra small Surface-Mounted Device (SMD)
- Size 1 mm x 0.6 mm x 0.39 mm (0402)



## 1.2 Application Examples

- Reliable ESD and surge protection of highly susceptible IC/ASICs in computers and peripherals, audio, headset, human digital interfaces, video equipment, cellular handsets and accessories and portable electronics
- Dedicated solution to boost ESD and surge protection performance in miniaturized modern electronics
- 10/100/1000 Ethernet

## 1.3 Product Description

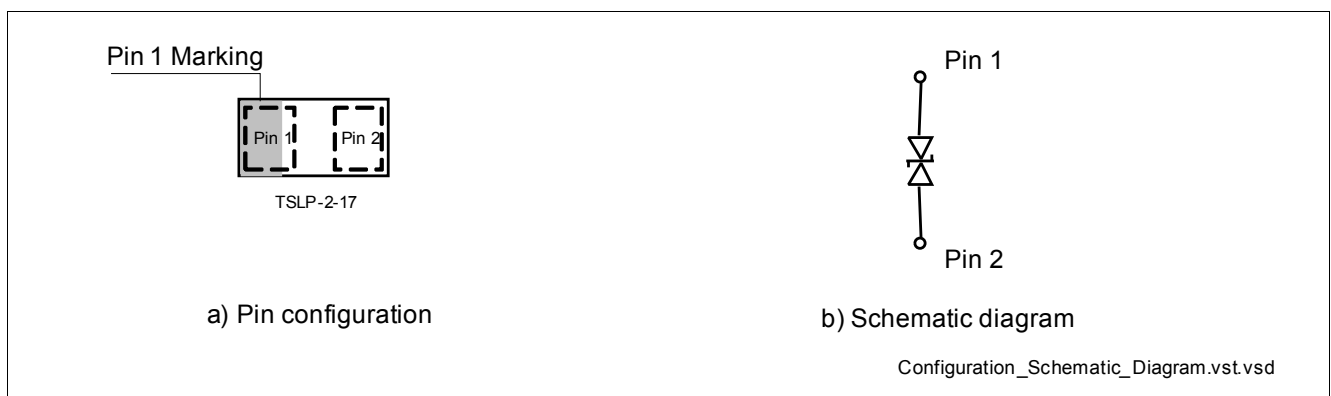


Figure 1-1 Pin Configuration and Schematic Diagram

Table 1-1 Ordering Information

Type	Package	Configuration	Marking code
ESD300-B1-02LRH	TSLP-2-17	1 line, bi-directional	S3



**Table 2-2 DC Characteristics at  $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise specified**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Reverse working voltage	$V_{RWM}$	-3.3	-	3.3	V	
Reverse current	$I_R$	-	-	100	nA	$V_R = 3.3\text{ V}$

**Table 2-3 RF Characteristics at  $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise specified**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Line capacitance	$C_L$	-	1.2	1.8	pF	$V_R = 0\text{ V}, f = 1\text{ MHz}$

**Table 2-4 ESD Characteristics at  $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise specified**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Clamping voltage <sup>1)</sup>	$V_{CL}$	-	8	-	V	$V_{ESD} = 8\text{ kV}, t_p = 30\text{ ns}$ contact discharge
Clamping voltage <sup>2)</sup>	$V_{CL}$	-	5	-	V	$t_p = 8/20\text{ }\mu\text{s}$ $I_{PP} = 1\text{ A}$ $I_{PP} = 12\text{ A}$ $I_{PP} = 18\text{ A}$
		-	8.5	-		
		-	10.5	-		
Clamping voltage <sup>3)</sup>	$V_{CL}$	-	9.5	-	V	$t_p = 100\text{ ns}$ $I_{PP} = 16\text{ A}$ $I_{PP} = 30\text{ A}$
		-	12.5	-		
Dynamic resistance <sup>3)</sup>	$R_{DYN}$	-	0.23	-	$\Omega$	

1)  $V_{ESD}$  according to IEC61000-4-2 ( $R = 330\text{ }\Omega, C = 150\text{ pF}$  discharge network)

2)  $I_{PP}$  according to IEC61000-4-5 ( $t_p = 8/20\text{ }\mu\text{s}$ )

3) ANSI/ESD STM5.5.1 - Electrostatic Discharge Sensitive Testing using Transmission Line Pulse (TLP) Model. TLP conditions:  $Z_0 = 50\text{ }\Omega, t_p = 100\text{ ns}, t_r = 0.6\text{ ns}, I_{TLP}$  and  $V_{TLP}$  averaging window:  $t_1 = 30\text{ ns}$  to  $t_2 = 60\text{ ns}$ , extraction of dynamic resistance using least squares fit of TLP characteristic between  $I_{TLP1} = 10\text{ A}$  and  $I_{TLP2} = 40\text{ A}$ . Please refer to Application Note AN210 [1]

Typical Characteristics at  $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise specified

### 3 Typical Characteristics at $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise specified

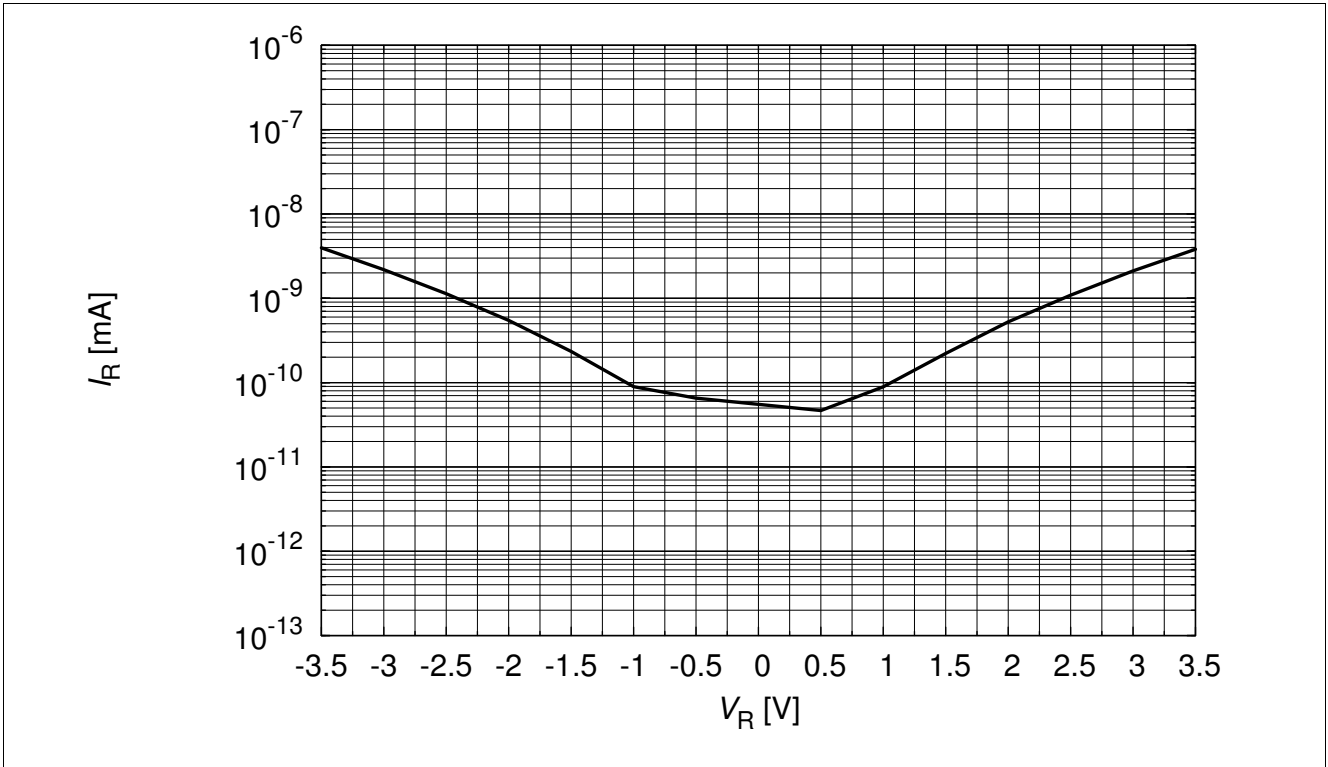


Figure 3-1 Reverse current:  $I_R = f(V_R)$

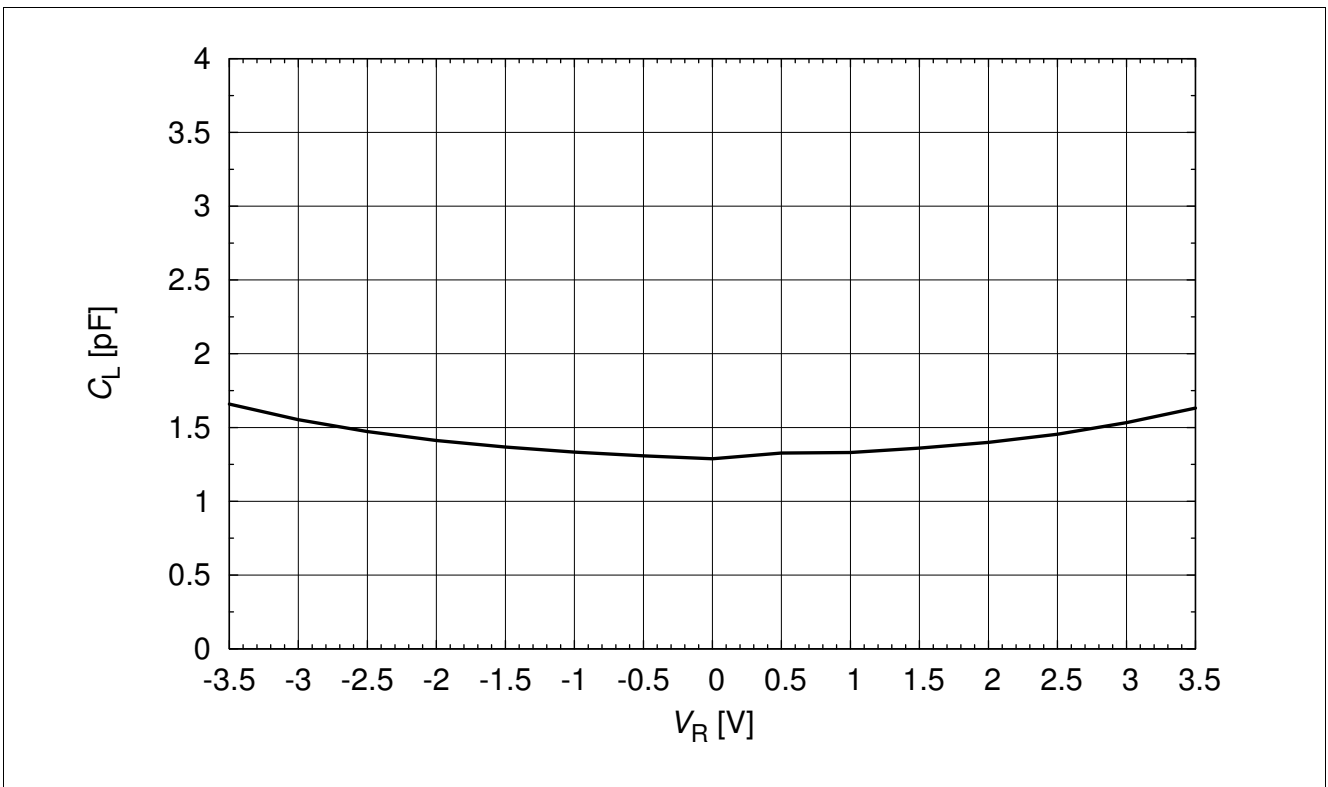
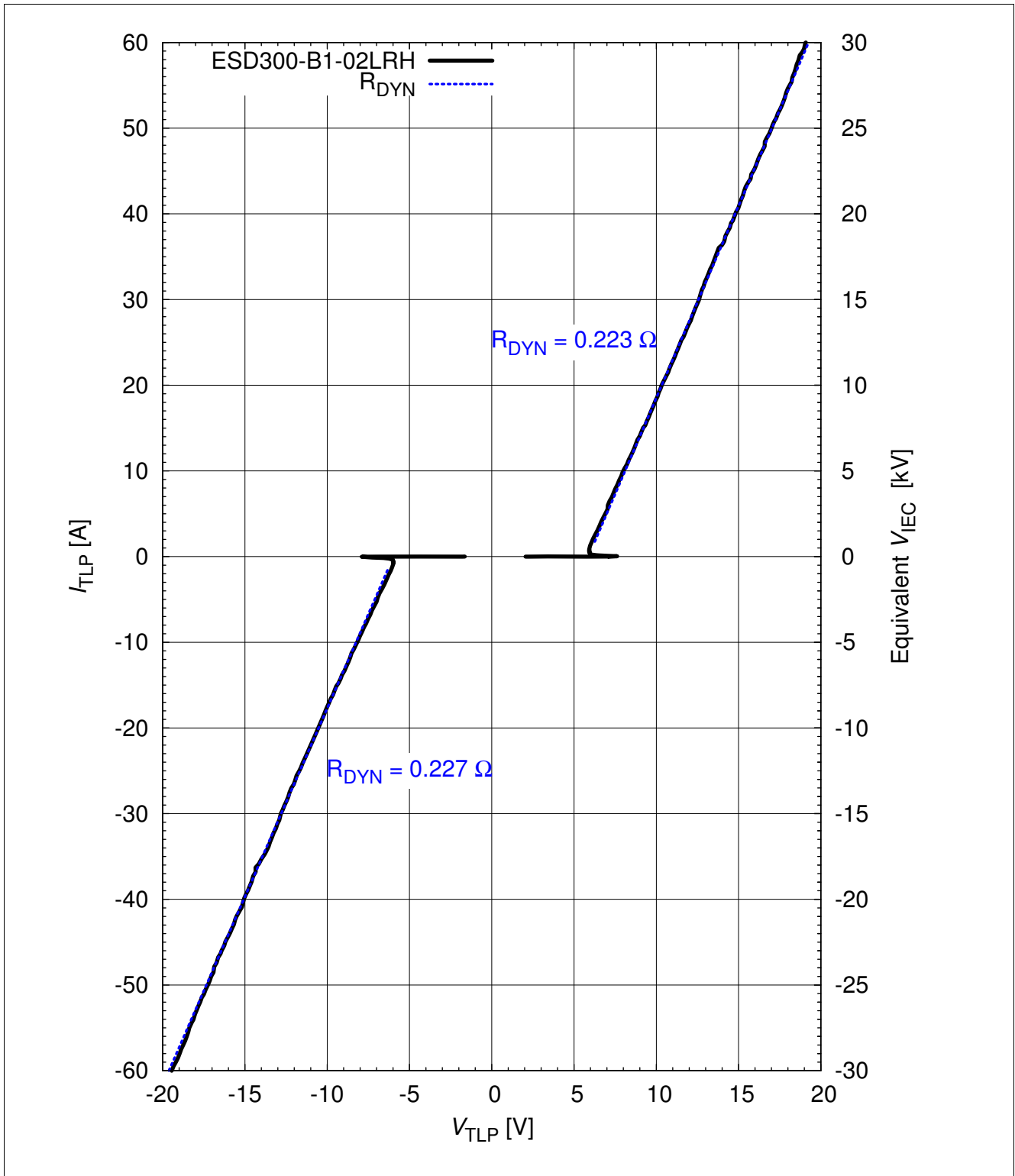


Figure 3-2 Line capacitance:  $C_L = f(V_R), f = 1\text{ MHz}$

Typical Characteristics at  $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise specified



**Figure 3-3 Clamping voltage (TLP):  $I_{TLP} = f(V_{TLP})$  according ANSI/ESD STM5.5.1 - Electrostatic Discharge Sensitivity Testing using Transmission Line Pulse (TLP) Model. TLP conditions:  $Z_0 = 50\ \Omega$ ,  $t_p = 100\text{ ns}$ ,  $t_r = 0.6\text{ ns}$ ,  $I_{TLP}$  and  $V_{TLP}$  averaging window:  $t_1 = \text{ns}$  to  $t_2 = 60\text{ ns}$ , extraction of dynamic resistance using squares fit to TLP characteristics between  $I_{TLP1} = 10\text{ A}$  and  $I_{TLP2} = 40\text{ A}$ . Please refer to Application Note AN210 [1]**

Typical Characteristics at  $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise specified

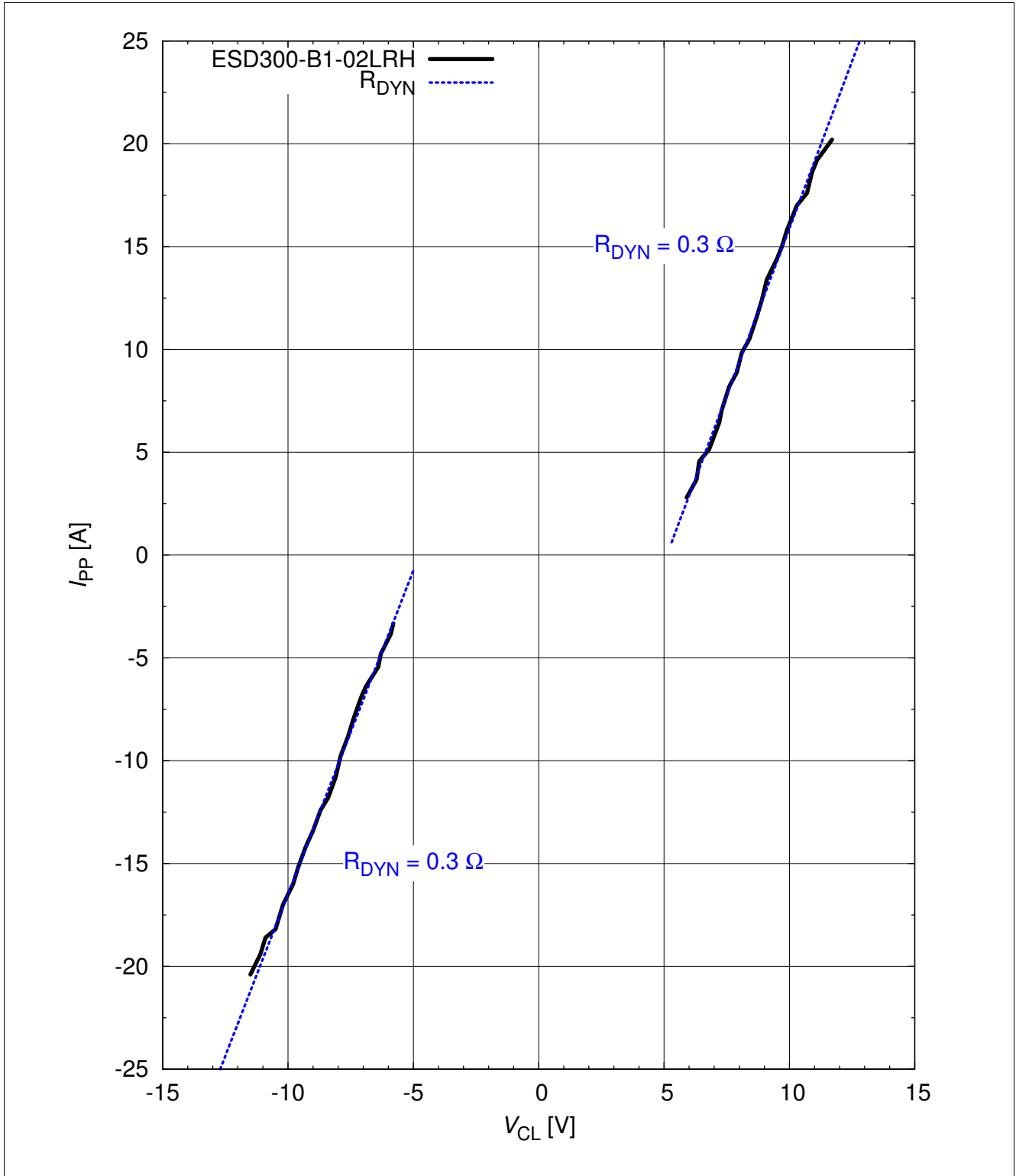


Figure 3-4 Pulse current (IEC61000-4-5) versus clamping voltage:  $I_{PP} = f(V_{CL})$



Typical Characteristics at  $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise specified

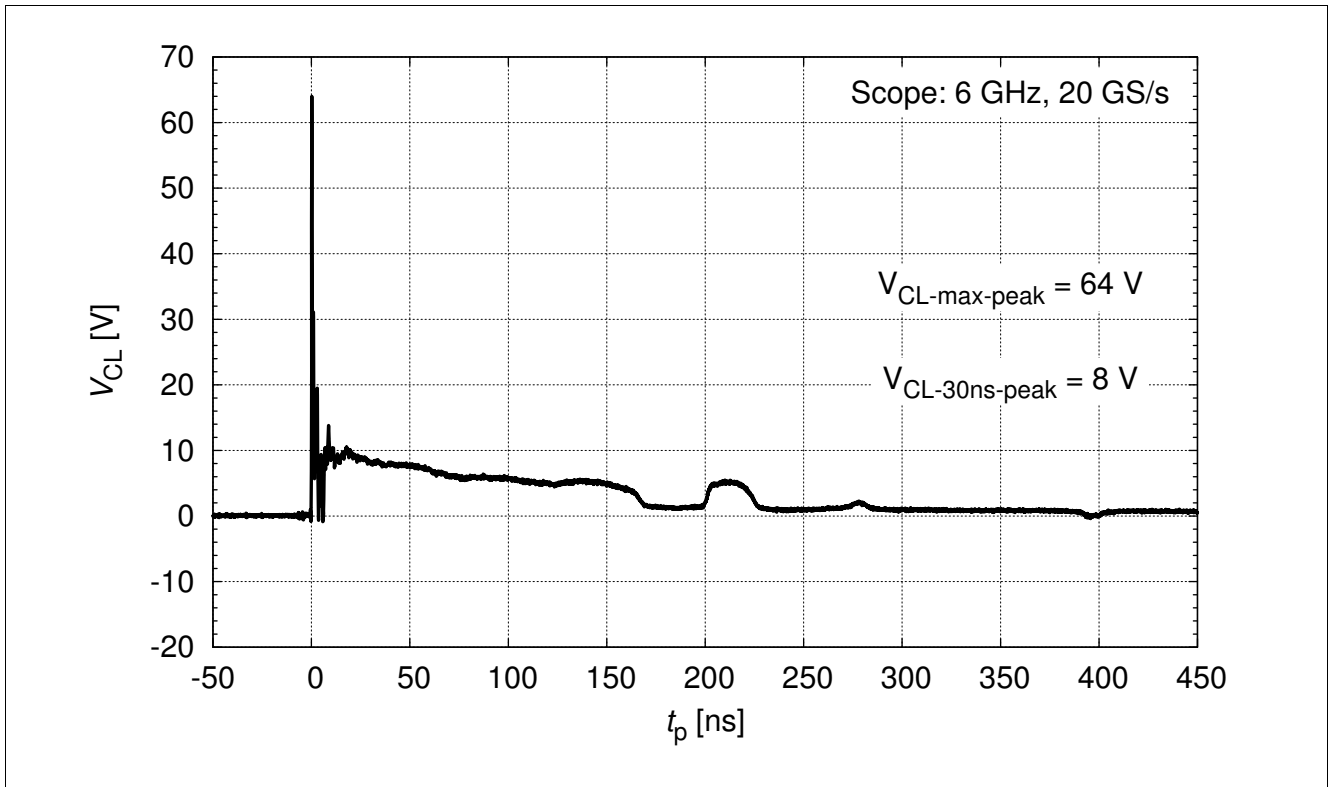


Figure 3-5 IEC61000-4-2 :  $V_{CL} = f(t)$ , 8 kV positive pulse from pin 1 to pin 2

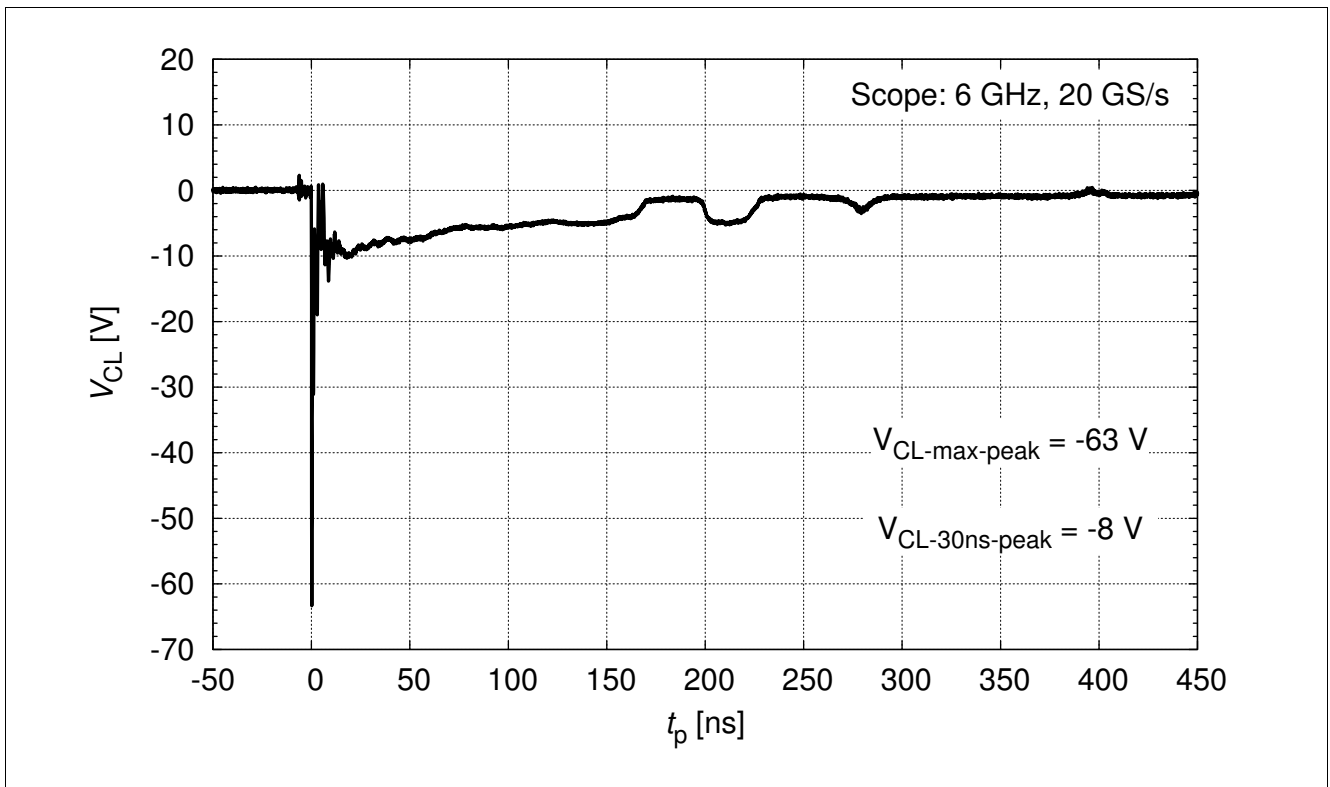


Figure 3-6 IEC61000-4-2 :  $V_{CL} = f(t)$ , 8 kV negative pulse from pin 1 to pin 2

Typical Characteristics at  $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise specified

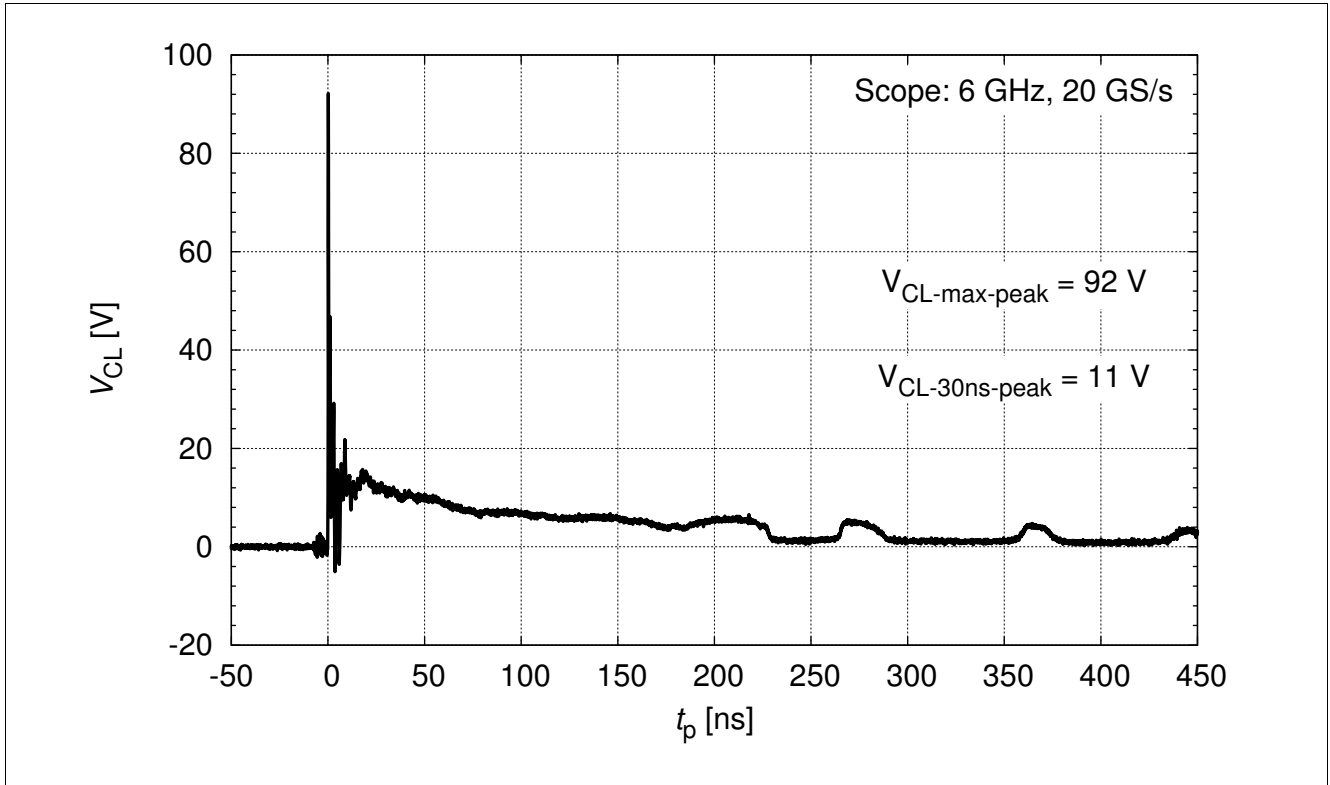


Figure 3-7 IEC61000-4-2 :  $V_{CL} = f(t)$ , 15 kV positive pulse from pin 1 to pin 2

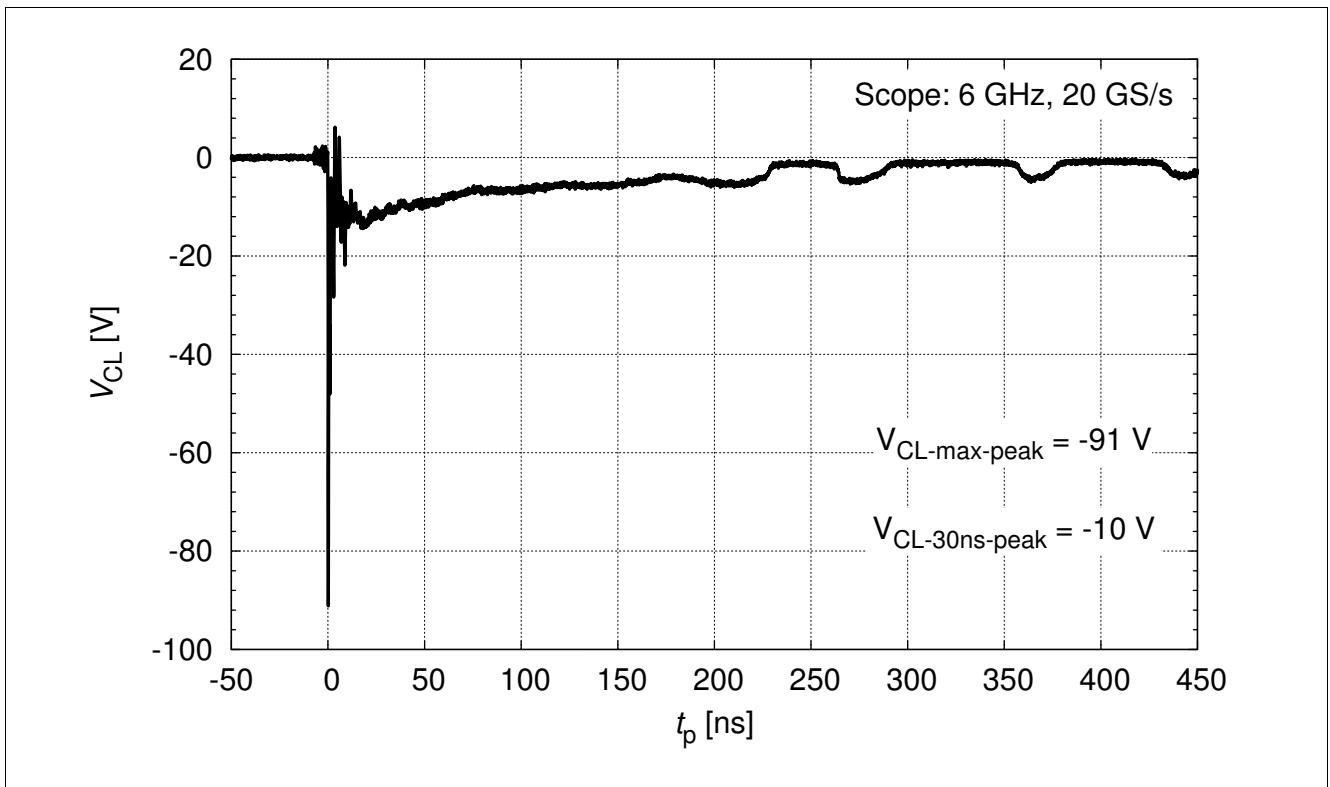


Figure 3-8 IEC61000-4-2 :  $V_{CL} = f(t)$ , 15 kV negative pulse from pin 1 to pin 2

## 4 Package Information

### 4.1 TSLP-2-17

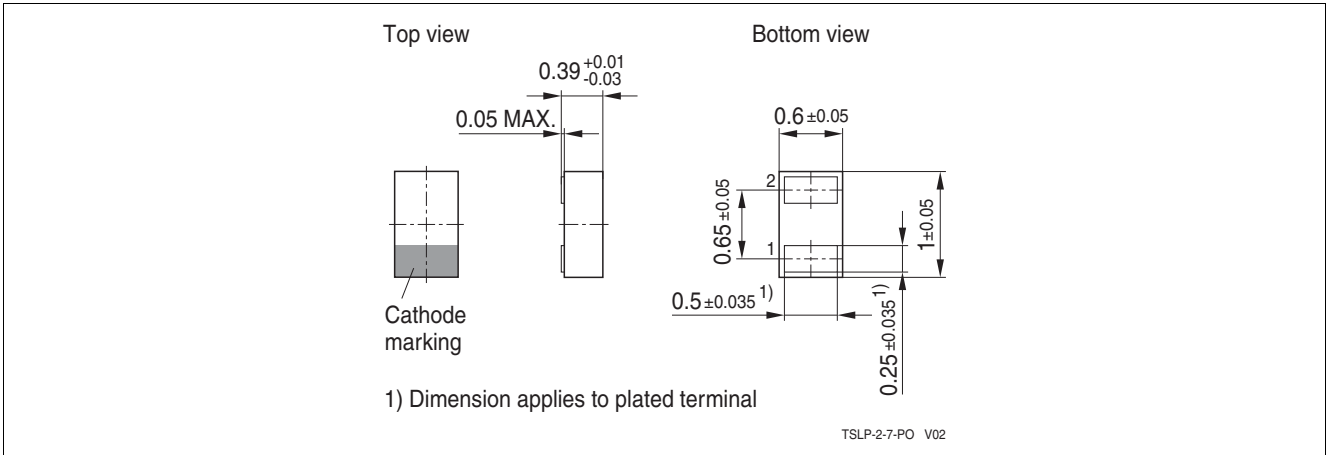


Figure 4-1 TSLP-2-17 Package outline (dimension in mm)

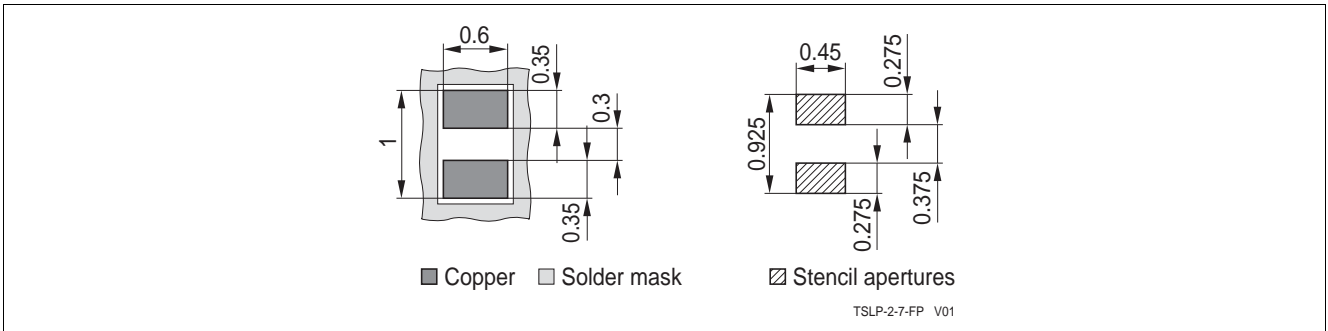


Figure 4-2 TSLP-2-17 Footprint (dimension in mm)

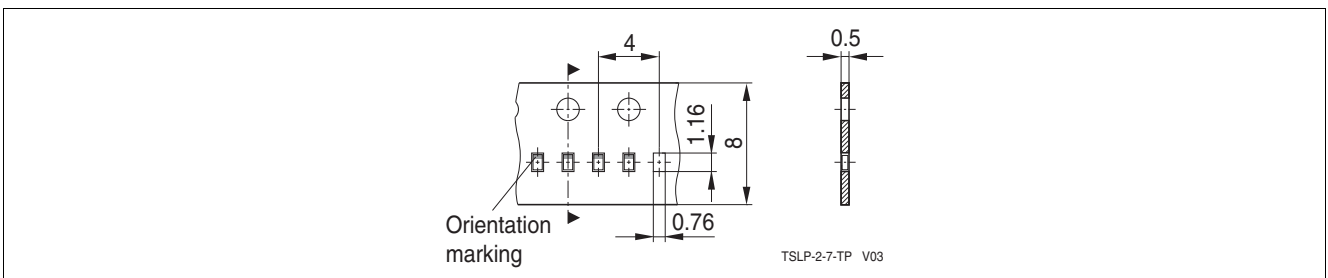


Figure 4-3 TSLP-2-17 Packing (dimension in mm)

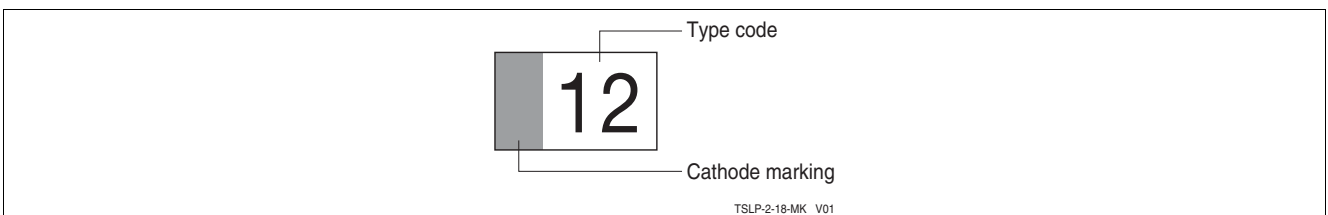


Figure 4-4 TSLP-2-17 Marking (example)

**References**

- [1] Infineon AG - **Application Note AN210**: Effective ESD Protection design at System Level Using VF-TLP Characterization Methodology

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