APPLICATION NOTE

UHF Transmitter IC ATA5749

ATA5749

Introduction

With the new UHF transmitter ATA5749 Atmel® offers an optimized solution for unidirectional access systems. The transmitter is primarily designed for automotive applications such as Tire Pressure Monitoring Systems (TPMS), Remote Key-less Entry (RKE) and Passive Entry Go (PEG). In addition the ATA5749 can also be used for any access and remote control system in industrial applications. This application note provides technical background information which helps to quickly understand and apply the device.

General Description

The ATA5749 is an integrated fractional-N-PLL transmitter that operates in the Industrial Scientific and Medical (ISM) frequency band. The IC transmits signals with Amplitude Shift Keying (ASK) and Frequency Shift Keying (FSK) modulation with a data rate of up to 40kBits/s in Manchester coding. Several features can be set by using the SPI interface, for example, the operating frequency in the range of 300MHz to 450MHz and the transmit power in the range of –0.5dBm to +12.5dBm. To ensure maximum battery lifetime the transmitter features low current consumption, for example, just 7.3mA at 5.5dBm output power (typical). Due to the small-sized TSSOP10 package only few external elements are needed to realize an end application with minimum board space consumption (please refer to Figure 1-1 on page 3).

Figure 1 shows the Pinning of the ATA5749, whereas the pin description is listed in Table 1.

Figure 1. ATA5749 Pinning

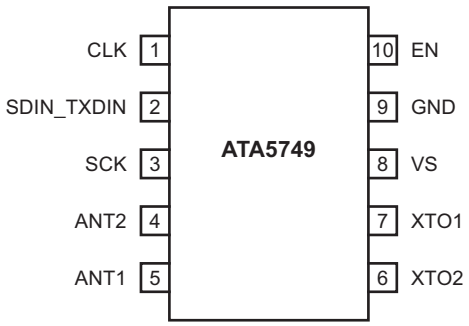


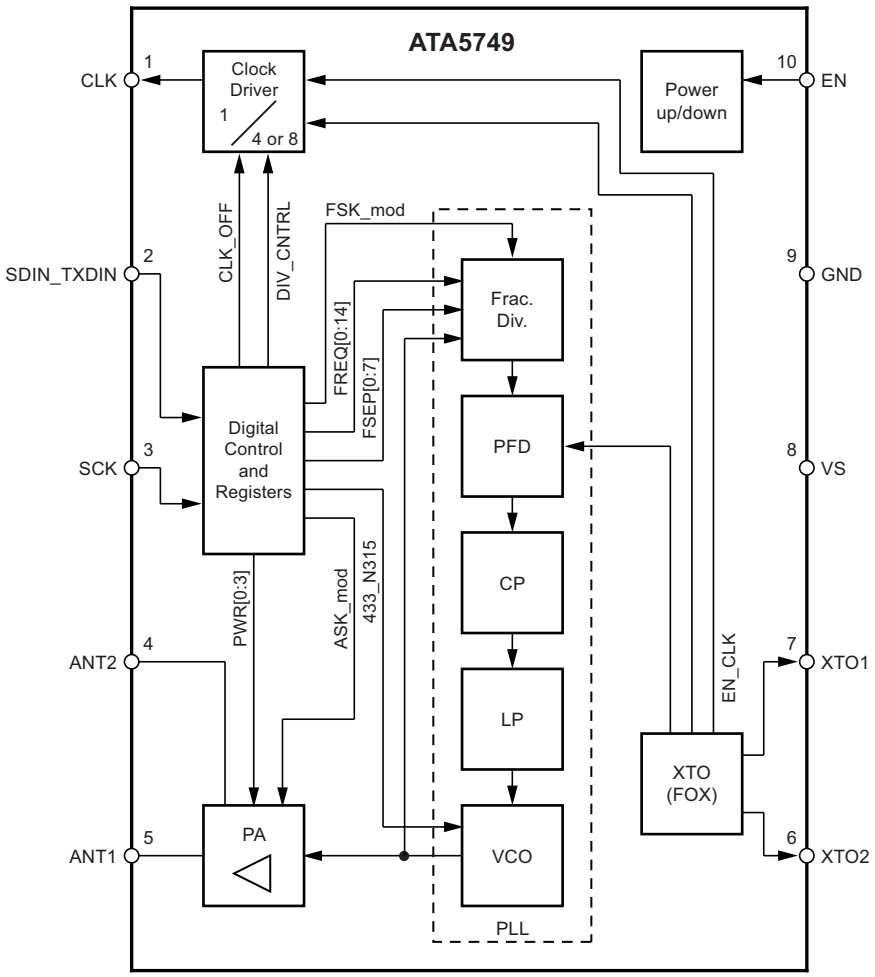
Table 1. ATA5749 Pin Description

Pin	Symbol	Function
1	CLK	CLK output
2	SDIN_TXDIN	Serial bus data input and TX data input
3	SCK	Serial bus clock input
4	ANT2	Antenna interface
5	ANT1	Antenna interface
6	XTO2	Crystal/C_{LOAD2} connection
7	XTO1	Crystal/C_{LOAD1} connection
8	VS	Supply Input
9	GND	Supply GND
10	EN	Enable input

1. Circuit Block Descriptions

This section describes the individual circuit blocks, providing more detailed information than in the ATA5749 datasheet. Figure 1-1 illustrates the transmitter's system block diagram.

Figure 1-1. System Block Diagram



1.1 Crystal Oscillator (XTO)

This block is based on the Pierce oscillator circuit with an amplitude regulation. The definition of the crystal oscillator's features and functionality is fixed. To start the crystal oscillator, pin EN must be set. The amplitude detector, which is implemented in the crystal oscillator block, monitors the oscillation amplitude. If the defined amplitude is reached, an internal signal bit XTO_RDY will be set (see Figure 1-1) and the clock output (pin CLK) will be switched on.

This method has two benefits. First it guarantees a stable PLL reference frequency and an optimum clock frequency accuracy. Second, the parasitic coupling from the clock output signal to the crystal oscillator pins (XTO1 and XTO2) - which may disturb the start-up process of the crystal oscillator - will not be critical since the clock output signal will be generated only if the oscillation amplitude is high enough. Nevertheless, the board layout must be designed properly to minimize parasitic coupling between the CMOS output of the pin CLK and the crystal oscillator.

The time period between the activation of the IC (EN='HIGH') and the output of the clock signal is defined as the crystal oscillator's start-up time, which mainly depends on the crystal's motional capacitance (Cm). The typical value of 200µs can be obtained using a crystal with a motional capacitance (Cm) of 4fF and a shunt capacitance (C0) of 1.5pF. The higher the motional capacitance (Cm) the faster the crystal oscillator's start-up.

The ATA5749's crystal oscillator features a high oscillation margin (negative resistance) of typically R_{XTO12_START} > 1500. This helps to reduce the failure rates caused by sleeping crystal phenomena. The external load capacitors must be selected so that the XTO oscillates on the loaded resonance frequency of the specified crystal. To ensure the specified start-up behavior and a low XTO current consumption it is recommended to choose a crystal with a load capacitance (CL) of 9pF.

1.2 Fractional-N PLL (Phase-locked Loop)

The Table 3-1 and Table 3-2 in Section 3. "ANNEX" on page 21 show the ATA5749's register configuration. The configuration of FREQ[0:14], FSEP[0:7] and *S434_N315* influences the frequency generated by the PLL block (please refer to Figure 1-1 on page 3). The ATA5749 provides two different VCO tuning ranges: 300MHz to 368MHz, and 367MHz to 450MHz. As can be seen in Table 1-1, the bit *S434_N315* in the register sets the VCO's RC oscillator and the fractional divider of the PLL.

Table 1-1. Bit *S434_N315* Configuration

S434_N315	ATA5749 Frequency Range
LOW	300MHz to 368MHz
HIGH	367MHz to 450MHz

In case of FSK modulation the carrier frequency will be internally modulated by *FSK_mod* Signal, which is identical to the available signal on the pin *SDIN_TXDIN*.

Table 1-2 shows the calculation of the RF output frequency based on the setting of FREQ[0:14], FSEP[0:7], *S434_N315* and the value of FSK_mod (*SDIN_TXDIN*).

Table 1-2. RF Output Frequencies' Calculation Based on the Register Setting

	S434_N315 = 'LOW'	S434_N315 = 'HIGH'
$f_{TX\_FSK\_mod='LOW'}$	$\left[24 + \frac{(FREQ + 0.5)}{16384}\right] \times f_{XTO}$	$\left[32.5 + \frac{(FREQ + 0.5)}{16384}\right] \times f_{XTO}$
$f_{TX\_FSK\_mod='HIGH}$	$\left[24 + \frac{(FREQ + FSEP + 0.5)}{16384}\right] \times f_{XTO}$	$\left[32.5 + \frac{(FREQ + FSEP + 0.5)}{16384}\right] \times f_{XTO}$
$f_{DEV\_\_FSK}$	$\frac{FSEP}{32768} \times f_{XTO}$	$\frac{FSEP}{32768} \times f_{XTO}$
f_{RF} (1)	$\left[24 + \frac{\left(\frac{FREQ + FSEP}{2} + 0.5\right)}{16384}\right] \times f_{XTO}$	$\left[32.5 + \frac{\left(\frac{FREQ + FSEP}{2} + 0.5\right)}{16384}\right] \times f_{XTO}$

Note: 1. The ASK carrier is corrected by adding FSEP/2 to FREQ for ASK transmission. If FSEP is an odd number, the FSEP/2 value is rounded to the lower next integer value, therefore, the ASK center frequency may differ to the FSK center frequency by 396Hz.

Definition:

- In ASK modulation f_{RF} is the center frequency of the transmitted signal.
- In FSK modulation f_{RF} is the virtual carrier that is defined using the Mark and Space Frequencies,

$$f_{RF} = \frac{f_{Mark} + f_{Space}}{2}$$

- $F_{Space} = f_{TX\_FSK\_mod='0'}$
- $f_{Mark} = f_{TX\_FSK\_mod='1'}$

The values to be used for FSEP are in the range of 1 to 255. Based on a crystal frequency ($f_{XTAL} = f_{XTO}$) of 13.0MHz the frequency deviation (f_{DEV_FSK}) is programmable within a range of ±396Hz to ±101.16kHz with a resolution of ±396Hz. For example, an FSK spectrum with a frequency deviation (f_{DEV_FSK}) of ±39.6kHz can be generated using *FSEP* = 100 and f_{XTO} = 13.0MHz as reference.

For proper system operation, the frequency setting of the fractional N-PLL must be well considered due to the fractional spurious emissions. With regard to the ATA5749, the FREQ values setting must be chosen in a range of 2500 to 22000.

The device can be operated at two standard operating frequencies in the ISM band, 315MHz and 433.92MHz, using one single crystal frequency of 13.0MHz (please refer to Table 1-2).

Table 1-3. Calculation of the Operating Frequencies in the 315 MHz and the 433.92 MHz Band Using 13.0 MHz Crystal Frequency

315.0MHz - Transmitter Application	433.92MHz - Transmitter Application
FREQ[0:14] = 3730 FSEP[0:7] = 100 S434_N315 = 0	FREQ[0:14] = 14342 FSEP[0:7] = 100 S434_N315 = 1
--> f_{RF} = 24.2307434 × f_{XTO} = 24.2307434 × 13MHz --> f_{RF} = 314.99966MHz	--> f_{RF} = 33.3784485 × f_{XTO} = 33.3784485 × 13MHz --> f_{RF} = 433.91983MHz
The frequency resolution is 793Hz	

The locking time of the PLL is defined, as follows

$$T_{PLL} = \frac{1280}{f_{XTO}}$$

The crystal frequency (f_{XTAL}= f_{XTO}) of 13.0MHz results in a PLL locking time (T_{PLL}) of 98.46µs. The PLL starts with the clock output activation (please refer to Figure 1-8 on page 12). The power amplifier and thus the data transmission can be started 98.46µs after the clock output activation. The typical start-up time of the crystal oscillator (XTO) is 200µs (DT_{XTO}). The reduced start-up time of PLL plus XTO (approximately 300µs) allows a short time delay between switching the transmitter on (EN = “HIGH”) and the beginning of the data transmission, which is important when designing a transmitter with low current consumption.

Notes:
1. The PLL will be started when the internal signal XTO_RDY is set and the programming of the 32-bit register (see Figure 1-8 on page 12 and Figure 1-9 on page 12) has been completed successfully.
2. In case the register programming by the microprocessor takes longer than the XTO start-up time (DTXTO), the PLL will start after the last bit has been programmed into the 32-bit register (see Figure 1-9 on page 12 and Figure 3-1 on page 22).

This programmable feature using the control bit *FREQ[0:14]* enables the correction of crystal tolerances and the application of frequency channeling.

1.3 Clock Output Driver (CLK_DRV)

The bit *DIV_CNTRL* determines the clock frequency generated by the transmitter. If bit *DIV_CNTRL* is set, the generated clock frequency is the crystal oscillator's frequency (f_{XTO}) divided by 4, whereas the division factor for the clock frequency is 8 if bit *DIV_CNTRL* has been cleared. Using a 13.0-MHz crystal, the clock frequencies of 1.625MHz or 3.25MHz will be generated according to the setting of DIV_CNTRL. The generated clock signal (pin CLK) is CMOS compatible and can drive load capacitances of up to 20pF at a frequency of 1.625MHz, and up to 10pF at a frequency of 3.25MHz.

Bit CLK_ON controls the activation of both the clock output and the internal signal XTO_RDY (please refer to Section 1.1 “Crystal Oscillator (XTO)” on page 3). If CLK_ON is cleared the IC does not generate any clock signal at pin CLK, resulting in a lower current consumption. During power-down mode the pin CLK remains on low level. The low level on the pin CLK will change if the amplitude of the crystal oscillator is sufficiently large (XTO_RDY is set). Hence the clock output and the internal XTO_RDY signal are always synchronized. With this synchronization spikes during the activation of the clock output will be avoided, because the clock signal always starts with a full period.

The transmitter ATA5749 offers a clock-only mode where only the crystal oscillator and the clock driver are active. Setting the CLK_Only bit will cause the transmitter to switch to clock-only mode.

1.4 Power Amplifier (PA)

To activate the power amplifier, the PLL needs to be locked and the internal signal XTO_RDY must be set (please refer to Section 1.2 “Fractional-N PLL (Phase-locked Loop)” on page 4). The PA’s output power can be programmed in a range of –0.5 dBm to 12.5 dBm by setting the PWR[0:3] bits in the register (please refer to Table 1-1 on page 4 and Table 1-2 on page 4). In ASK mode the transmitter frequency will be corrected to the center of the FSK, see Table 1-2 on page 4 and the PA will be modulated by the internal ASK_mod signal, which is equal to the data (signal) on the pin SDIN_TXDIN.

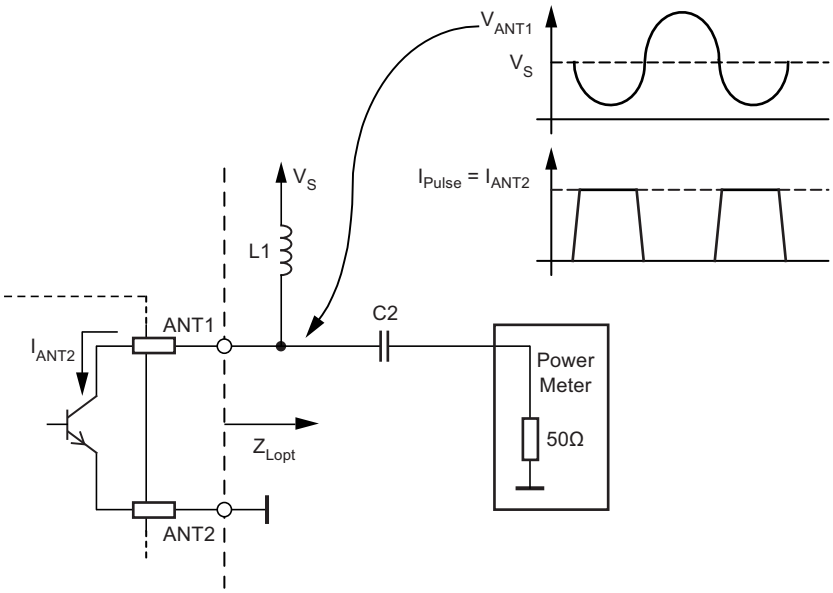
1.4.1 Class-C Power Amplifier

The power amplifier is designed as a class-C amplifier. This kind of circuit delivers current pulses at the open-collector output which is almost independent from the load impedance, supply voltage and temperature. Another advantage of this architecture is a relatively simple matching to an antenna or to a 50Ω load. Figure 1-2 on page 6 shows how the class-C PA basically works.

The required output power can be chosen by setting the PWR[0:3] bits in the register (see Table 3-1 and Table 3-2 on page 21). This setting adjusts the peak value of the current pulses (I_{Pulse}), delivered by the PA. That way the current consumption for pre-specified RF output power can be optimized to obtain the best possible PA efficiency.

During production the peak value of I_{Pulse} is calibrated to guarantee that variations due to production tolerances do not exceed ±10%. This results in a tight tolerance of the PA current and thus of the ATA5749’s output power. For each power setting an output power variation of ±1.5dB (including production tolerance) can be expected.

Figure 1-2. Operating Principle of Class-C PA



Since the PA’s efficiency depends on the PA’s load impedance, the matching elements must be optimized for every power setting to achieve the optimum load impedance (Z_{LOPT}), see Figure 1-2 on page 6.

For example:

Load impedance Z_{LOPT} = (180+j300)Ω at 315MHz operating frequency

Power supply V_S = 3V

Output power setting PWR[0:3]=8, which defines the output power of 5.5dBm at 50Ω

In this example, the PA’s current consumption will be typically 3.6mA and thus 7.3mA for the entire transmitter. This results in an power amplifier efficiency (PAE) of 32%.

In case of an optimum load, an efficiency of η_{PA} = 26% can be achieved with a 1.2-dBm power setting (PWR[0:3]=4), and η_{PA} = 36% with a maximum output power setting of 12.5dBm (PWR[0:3]=15).

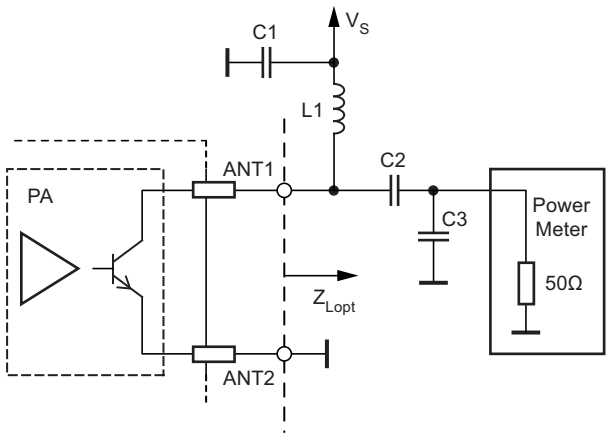
The load impedance is defined as the impedance of the matching network, or more specifically, the ratio between the RF voltage peak and the RF current peak at the power amplifier output (see Figure 1-2 on page 6). If the optimum load impedance (Z_{LOPT}) is obtained, the RF voltage amplitude will almost reach the supply voltage (please refer to Figure 1-2 on page 6). The 50Ω load matching method will be addressed in more detail in Section 1.4.2 “Output Matching to 50Ω Load” on page 7.

The ATA5749 is designed as a class-C power amplifier since this architecture provides significant advantages compared to other architectures such a class-E power amplifier, for example. Thanks to the class-C architecture the PA output is almost independent from the load impedance variation, which could increase the supply current and hence overload the battery of the transmitter module. In worst case, if the battery capacity is already at its limit, the transmitter’s supply volt-age drops drastically due to overload, which leads to a malfunction of the module. Please note that a hand approaching the antenna's area may also cause load impedance variations.

1.4.2 Output Matching to 50Ω Load

Figure 1-3 illustrates the basic measurement assembly of the output power matching to a 50Ω load. Table 1-1 on page 4 and Table 1-2 on page 4 show the power setting, the optimum achieved output power and the optimized values of the matching elements for each programmed output power. The matching element terms refer to Figure 1-3.

Figure 1-3. Principle of the Output Power Measurement Assembly



As mentioned in the last section an optimum power can be achieved if the peak amplitude value of the RF output voltage is close to the power supply (V_S). To this end, a low resistive path from the collector output of the PA to V_S supplies the necessary DC current. The inductor L1 is used as RF choke, connecting pin Ant1 to VS. To prevent coupling between the PA and the supply voltage, which may disturb PLL operation, the 1-nF decoupling capacitor C1 (X7R) must be placed as close as possible to the RF chokes and the power amplifier.

In case of an optimum load impedance (Z_{Lopt}), the PA’s output capacitance (approximately 0.7pF) and the board’s parasitic capacitance will be absorbed, and the PA delivers the RF current to a pure resistive load (R_{load}). In practice, the R_{load} value can be measured between pins ANT1 and ANT2. During R_{load} measurement the ATA5749 must be kept in OFF_Mode and must also remain soldered on the board.

It must be taken into account that the RF choke (L1) consists of a resistive part which causes a matching loss. This loss can be calculated using the following equation:

- Parallel equivalent resistance of an inductor

  $R_{Loss} = 2 \times \pi \times f_{RF} \times L_1 \times Q_{L1}$ Equation 3-1

- Mismatch loss

  $$10 \times \log\left(1 + \frac{R_{Lopt}}{R_{Loss}}\right)$$ Equation 3-2

Example how to calculate the matching loss:

- f_{RF} = 315MHz
- power setting PWR[0:3]=4
- R_{Load} = 1600Ω
- L_1 = 100nH (0805CS) with a Q factor of 45

--> The estimated matching loss will be 0.72dB.

Table 1-4. Measured PA Matching at 315 MHz with Typical Samples (50Ω, CLK_ON = 'Low')

Register PWR[0:3]	P_{target}/ dBm	L1/nH	C1/pF	C2/pF	R_{lopt}/Ω	Z_{lopt}/Ω	Assumption C_{par}/pF	Meas P/dBm
3	–0.5	110	1.2	1.6	2950	110+540j	0.9	–0.37
4	1	100	1.5		1940	150+520j	0.9	1.12
5	2.5	100	1.5		1550	190+520j	0.9	2.11
6	3.5	100	1.5		1250	220+480j	0.9	3.23
7	4.5	82	1.8		1000	240+430j	0.9	4.38
8	5.5	82	2.2		730	280+360j	0.9	5.42
9	6.5	68	2.7		580	290+300j	0.9	7.14
10	7.5	68	2.7		460	290+290j	0.9	8.22
11	8.5	68	3.3		350	280+225j	0.9	8.63
12	9.5	56	3.6		320	250+150j	0.9	9.79
13	10.5	47	4.7		250	215+85j	0.9	10.52
14	11.5	47	5.6		190	180+50j	0.9	11.67
15	12.5	47	5.6		160	160+45j	0.9	13

Table 1-5. Measured PA Matching at 433.92 MHz with Typical Samples (50Ω, CLK_ON = 'Low')

Register PWR[0:3]	P_{target}/ dBm	L1/nH	C1/pF	C2/pF	R_{lopt}/Ω	Z_{lopt}/Ω	Assumption C_{par}/pF	Meas P/dBm
3	–0,5	68	0.9	1.5	2800	60+400j	0.9	–0.62
4	1	56	2.7 + 2.2		1850	90+390j	0.9	1.3
5	2.5	56	1.2		1450	110+380j	0.9	2.73
6	3.5	47	1.8	5.6	1150	130+370j	0.9	3.03
7	4.5	47	1.6		950	150+350j	0.9	4.63
8	5.5	47	1.8		680	180+300j	0.9	6.18
9	6.5	43	2.2	1	560	200+270j	0.9	6.66
10	7.5	36	2.4		450	210+230j	0.9	7.91
11	8.5	33	3		340	200+170j	0.9	8.68
12	9.5	36	2.7		310	195+150j	0.9	9.8
13	10.5	36	3.6		230	175+100j	0.9	10.49
14	11.5	27	4.7		180	150+70j	0.9	11.6
15	12.5	27	4.7		150	130+50j	0.9	12.5

Notes to the Table 1-4 on page 8 and Table 1-5:

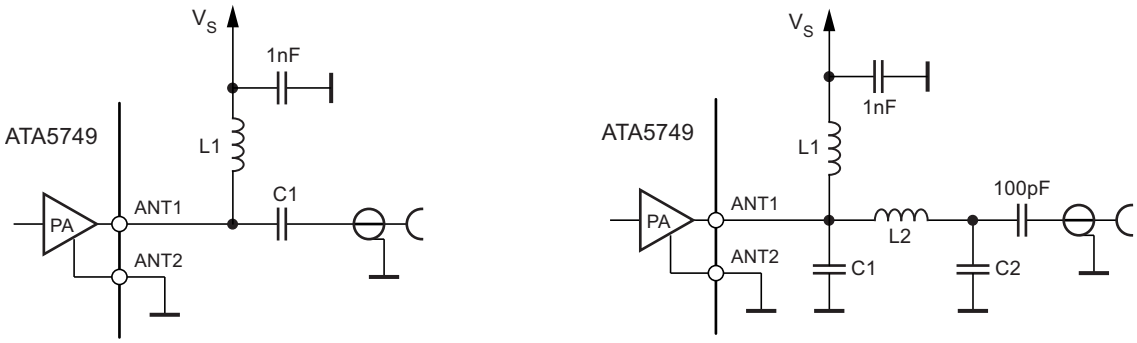
- The measured values in Table 1-5 are verified using Atmel's demo board ATAB5749.
- Used inductors: COILCRAFT 0805CS
- Used capacitors: AVX ACCU-P 0402

1.4.3 Harmonics Rejection

In some cases the matching as explained in Section 1.4.1 “Class-C Power Amplifier” on page 6 and Section 1.4.2 “Output Matching to 50Ω Load” on page 7 does not result in sufficient harmonic suppression, so that an additional low-pass filter needs to be implemented. This chapter describes how the harmonics rejection can be improved by the 50Ω load matching.

Figure on page 9 illustrates PA matching - section b with an additional low-pass filter, section a without low-pass filter. All values in this chapter refer to an ATA5749 application with a 12.5-dBm power setting at a transmit frequency of 433.92MHz. Table 1-3 on page 5 lists the different matching constellation referring to the circuit as shown in Figure 1-4b. The measurement results as listed in Table 1-4 on page 8 show a different harmonic rejection performance due to the different matching constellation (see Table 1-3 on page 5).

Figure 1-4. PA Matching to a 50Ω Load



a (without Low-pass Filter)

b (with Low-pass Filter)

Table 1-6. Matching Elements

	L1 (0603CS)	C1/pF	C2/pF	L2 (0603CS)
Original	27nH	4.7pF	n.m.	n.m.
M1	39nH	5.6pF	1.5pF	27nH
M2	18nH	10pF	1.5pF	39nH
M3	18nH	9.1pF	1.5pF	39nH
M4	18nH	8.2pF	1.5pF	39nH

Table 1-7. Harmonics Rejection

	P_{out}	Hs1	Hs2	Hs3	Hs4
Original	12.58dBm	–19.99dB	–18.43dB	–24.17dB	–23.16dB
M1	11.43dBm	–32.08dB	–43.27dB	> –50dB	> –50dB
M2	9.37dBm	–36.83dB	> –50dB	> –50dB	> –50dB
M3	10.47dBm	–37.93dB	–47.05dB	> –50dB	> –50dB
M4	11.48dBm	–40.25dB	–47dB	> –50dB	> –50dB

Notes to Table 1-3 on page 5 and Table 1-4 on page 8:

- Original matching structure without low-pass filter
- M1 = first matching constellation, M2 = second matching constellation, etc.
- P_{out} = measured transmit power at 433.92MHz
- Hs1 = suppression of the 1st harmonic, Hs2 = suppression of the 2nd harmonic, etc.

1.4.4 ATA5749 Frequency Pulling Effect in ASK Mode

Generally, ASK modulation is performed by switching the power amplifier according to the data rate. When using this method, the decoupling between the power amplifier and the VCO needs to be taken into account in the application. The decoupling measures must be performed internally as well as on the board layout. Otherwise, VCO frequency pulling, affected by the switching of the power amplifier, may occur. Nevertheless, the basic rules of PCB layout design must be observed. Figure 1-5 and Figure 1-6 on page 10 show that the ATA5749 on the Atmel demo board does not exhibit any frequency pulling, even if the maximum transmit power is +12.5dBm.

Figure 1-5. Spectrum of 40kHz ASK Modulation at P_{out} = 12.5dBm

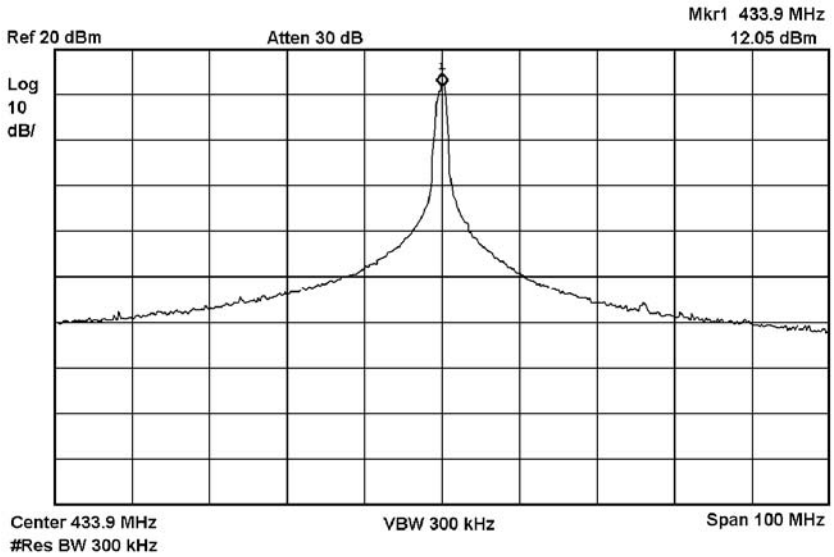
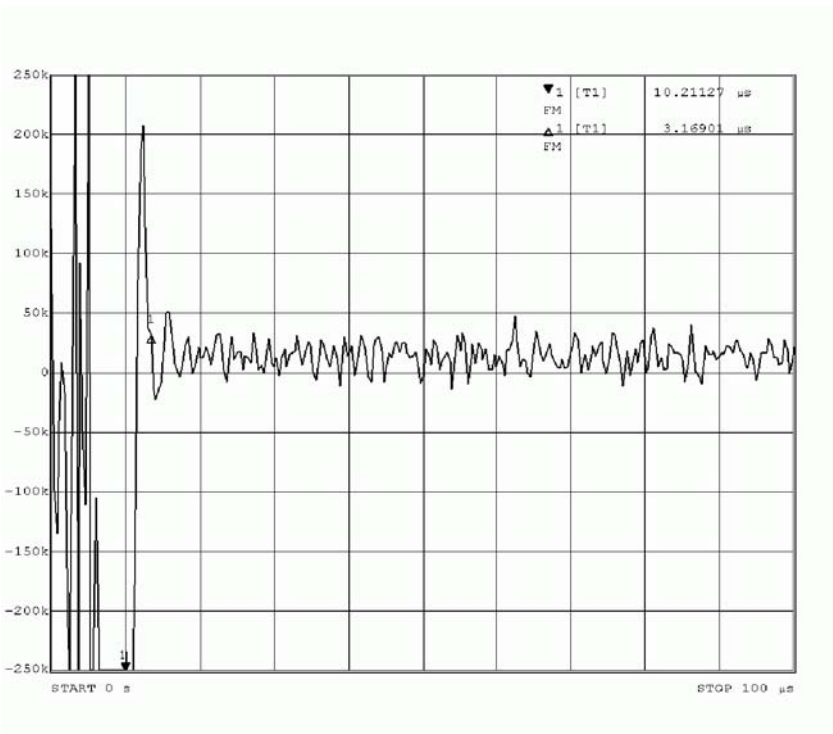


Figure 1-6. Demodulated RF Frequency during PA Switching at P_{out} = 12.5dBm



1.5 Timing of the Serial Peripheral Interface (SPI) Bus

The UHF transmitter ATA5749 incorporates an SPI bus for the configuration of the transmitter. This bus interface includes the following lines,

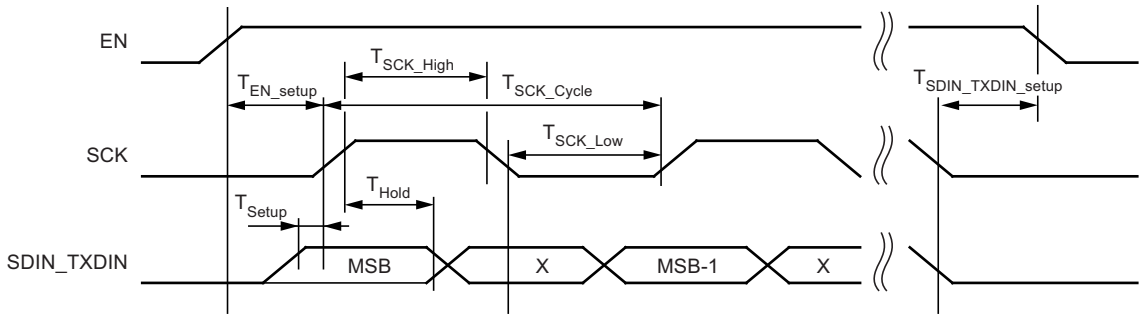
- Enable line (EN)
- Data line (SDIN_TXDIN)
- SPI bus clock (SCK)

SPI bus timing is illustrated in Figure 1-7 on page 11. The data applied on the SDIN_TXDIN will be transferred to the positive edge of the SPI clock. In addition to the programming functionality, pin SDIN_TXDIN also serves as modulating data input for ASK and FSK. The applied data on pin SDIN_TXDIN will be passed directly as an internal signal (either as ASK_mod or as FSK_mod, depending on the chosen modulation type, please refer to Figure 1-1 on page 3). The register bit ASK_NFSK set the modulation type (please see Table 3-1 and Table 3-2 on page 21). Pin SDIN_TXDIN will be released as data input if the programming of the 32-bit register has been completed. The timing of the register programming can be seen in Figure 1-8 on page 12 and Figure 1-9 on page 12.

More information on the SPI bus timing conditions can be found in the ATA5749 datasheet (section “Timing Characteristics”). If these conditions are met a maximum SPI bus clock speed of 2MHz can be achieved.

Note: During OFF_MODE pin SDIN_TXDIN and pin SCK must set to the ground.

Figure 1-7. SPI Bus Timing



1.5.1 Timing of Register Programming and Data Transmission

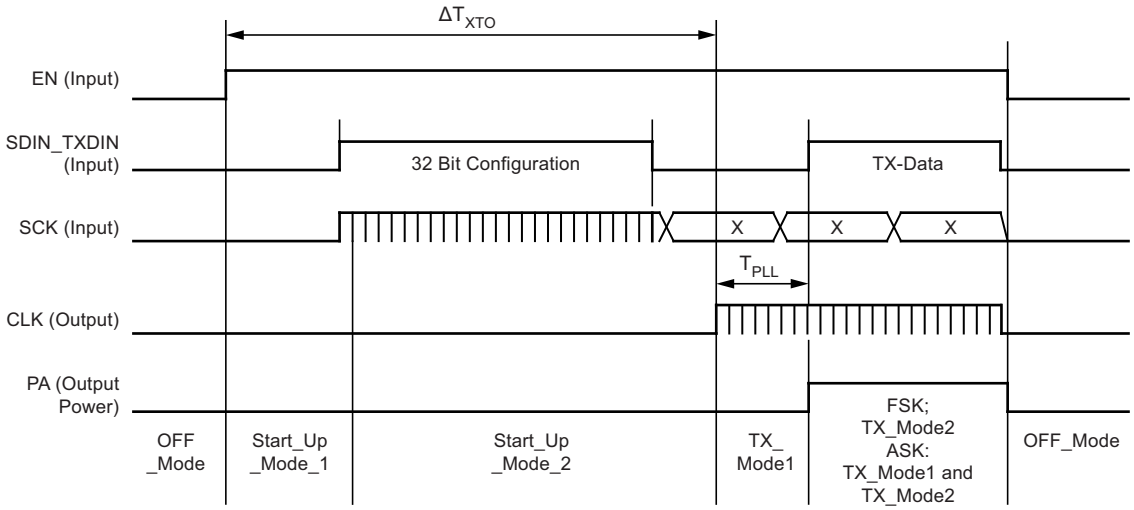
1.5.1.1 Timing if the Register Programming Sequence is Faster than XTO Start-up Time

If pin EN is set, the XTO starts immediately. During the start-up process the microprocessor sends the programming sequence (32 configuration bits) via the SPI interface. This programming sequence also needs to be synchronized to the clock frequency on pin SCK, which is usually generated by microprocessor’s internal RC oscillator. Figure 1-8 illustrates the programming sequence if the XTO start-up lags behind the programming speed. As mentioned in Section 1.1 “Crystal Oscillator (XTO)” on page 3 the transmitter ATA5749 will generate the clock signal with a crystal tolerance of 200µs typically (ΔTXTO) at pin CLK after switching on. That way the clock signal frequency is stable and can be used by the microprocessor as reference to generate the data rate. After a further delay of 98.46µs (T_{PLL}) the power amplifier will be activated automatically, and any telegram available at pin SDIN_TXDIN will be transmitted immediately.

During data transmission the microprocessor clock at pin SCK does not impact the transmitter’s functionality. To extend the battery lifetime the ATA5749 must be disabled after each data transmission. For this purpose the SPI interface needs to be cleared (EN = 0, SCK = 0 and SDIN_TXDIN = 0).

Note: This timing condition allows short data transmissions as the register programming sequences will be completed during the XTO’s start-up time.

Figure 1-8. Timing Diagram if Register Programming Sequence is Faster than ΔTXTO



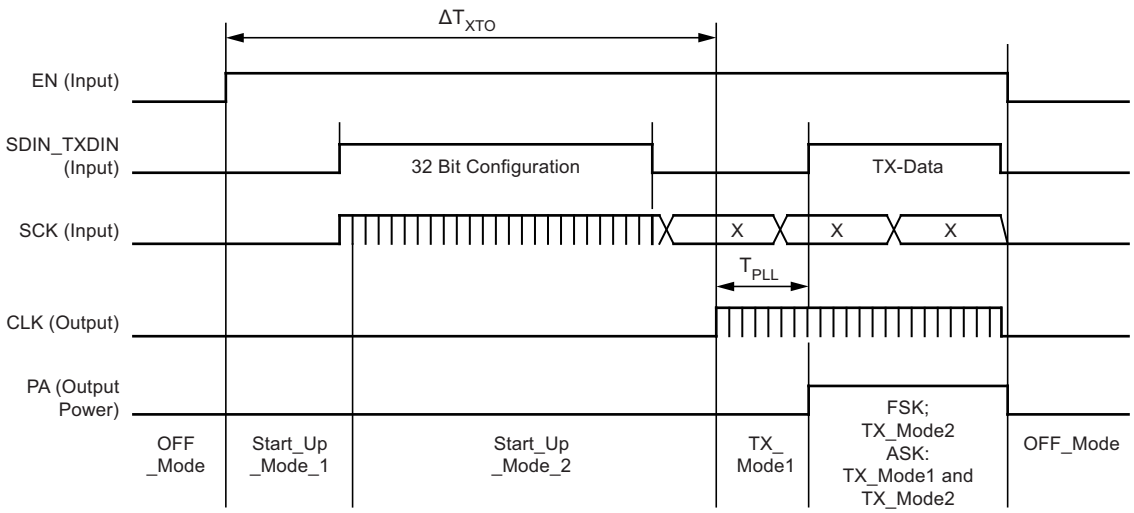
1.5.1.2 Timing if Register Programming Sequence is Slower than XTO Start-up Time

As described in Section 1.5.1.1 “Timing if the Register Programming Sequence is Faster than XTO Start-up Time” on page 11 the microprocessor sends the programming sequence (32 configuration bits) via the SPI interface. This programming sequence also needs to be synchronized to the clock frequency on pin SCK, which is usually generated by microprocessor’s internal RC oscillator.

If the SPI programming takes remarkably more time than the XTO start-up, the internal crystal oscillator signal reaches a stable condition earlier than the register programming sequence. In this case the clock signal at pin CLK will be generated exactly after the completion of the register programming progress. The next steps (PA activation, data transmission and switching-off the transmitter) are identical to those described in the previous section. Figure 1-9 illustrates the programming sequence if the XTO start-up is faster than the programming.

This method ensures exact timing for the microprocessor, regardless of the fact that the register programming takes longer than the XTO start-up.

Figure 1-9. Control Timing if Programming is Slower than T_{XTO}



Note: The register is programmed with the negative SCK edge of programming LSB

1.6 Clock Only Mode

This mode might be useful for specific applications where the clock frequency is still needed for the microprocessor as a reference while the other functional transmitter blocks are deactivated. This mode is controlled by the register bit CLK_Only, and only the XTO and the clock driver are active. The generated clock frequency depends on the division ratio controlled by the register bit DIV_CNTRL. For the clock functionality, bit CLK_ON must always be set, of course. The register contents are listed in Table 3-1 and Table 3-2 on page 21.

Figure 1-10. Control Timing CLK_Only_Mode if Register Programming is Faster than ΔTXTO

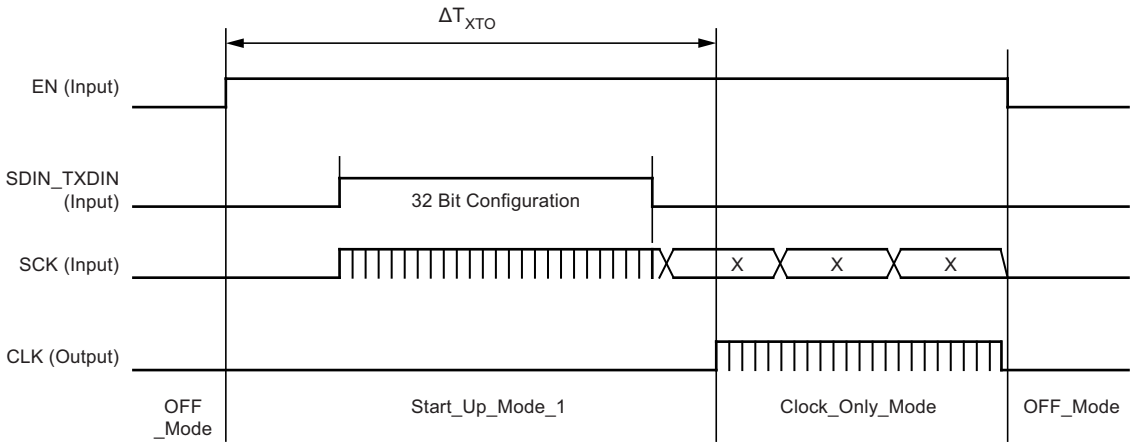
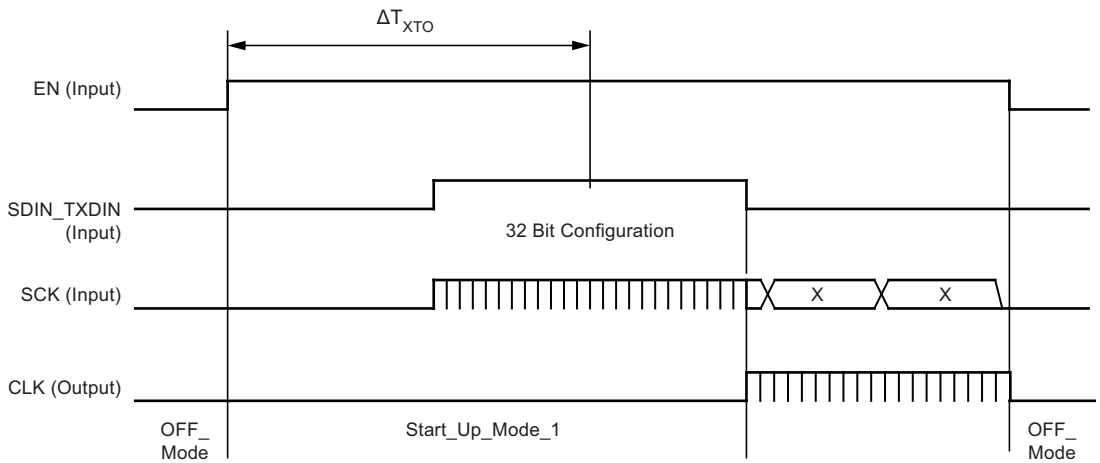


Figure 1-11. Control Timing CLK_Only_Mode if Register Programming is Slower than ΔTXTO



2. Application

2.1 Loop Antenna Design

The matching of the Power Amplifier to the 50Ω load is described in Section 1.4.2 “Output Matching to 50Ω Load” on page 7. This section focuses on applications using an antenna, especially a loop antenna. Different applications and operating frequencies need different antenna considerations. Short-range devices in the ISM (Industrial, Scientific and Medical, 315MHz, 433.92MHz and 868MHz) bands mainly use quarter-wave monopoles, helical antennas or printed small-loop antennas. The antenna characteristics such as directivity, gain, polarization, impedance, and bandwidth determine the application’s system performance. In addition to the technical requirements the cost is the most significant issue for mass production. Therefore, the decision on the antenna type to be used is always a compromise between cost, package dimension and technical considerations. Typically printed “small” loop antennas are used in hand-held devices of wireless control systems since they are - apart from board space - for free, and they are smaller than a whip or helical antenna. The performance of a loop antenna is sufficient for most system requirements where hand or body approach is not involved. When selecting the antenna type for a transmitter module, potential hand or body approach must always be considered.

2.2 Loop Antenna Design Theory

This application note addresses the basic technical information required when applying a “small” loop antenna as used on Atmel’s demo board. Any loop antenna with a total circumference of less than a fifth of the wavelength (λ/5) can be defined as a “small” loop antenna. Several antenna design books even define loop antennas with a circumference of approximately a tenth of the wavelength (λ/10) as small loop antennas.

A loop antenna is a magnetic antenna that needs a current flow through the loop to generate the required magnetic field for the radiation. The radiation of an antenna can be expressed as radiation resistance (R_{Rad}):

$$R_{Rad} \approx 31.2 \times 10^{3}\left(\frac{A^{2}}{\lambda^{4}}\right) \qquad \text{Equation 4-1}$$

Notes:
1. A = loop area in square meters
2. λ = wavelength in meter

The second essential parameter is the loss of the printed loop antenna. This can be derived from the theory of the skin depth under the assumption that the trace width is remarkably greater than the trace thickness. The loss resistance for a copper trace can be calculated using the following equation:

$$R_{loss\_loop} \approx \frac{1}{2w} \times (2.59 \times 10^{-7}) \times \sqrt{f} \qquad \text{Equation 4-2}$$

Notes:
1. L = the total perimeter of the antenna in meter referring to the trace’s centre
2. W = trace width in meter

In order to calculate the transmit power using the loop antenna it is necessary to determine the efficiency of the antenna. This is given by:

$$\eta = \frac{R_{Rad}}{R_{Rad} + R_{loss\_loop} + R_{loss\_cap}} \qquad \text{Equation 4-3}$$

Notes:
1. R_{Rad} = radiation resistance of the antenna
2. R_{loss_loop} = loss resistance of the loop’s trace
3. R_{loss_cap} = loss of the capacitors for the matching

The radiated power can be calculated, as follows

$P_{Rad} = I^{2}_{loop} \times R_{Rad}$ Equation 4-4

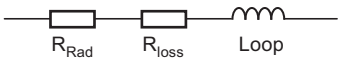
Note: I_{loop} = current flow through the loop antenna

The relation between the effective radiated power (ERP) and the transmitter output power ($P_{out,IC}$) driving the antenna:

$ERP = \eta \times P_{out,IC}$ Equation 4-5

The equivalent circuit for the loop antenna is useful during the matching progress (see Figure 2-1. The first step of the matching procedure is to determine the loop inductance. This value can be calculated using the formula for polygon inductance of a general shape (equation 4-6). The formula results in a relatively good accuracy of approximately ±5%. After that the Q factor of the antenna can be calculated using equation 4-7.

Figure 2-1. Equivalent Circuit of a Loop Antenna



$$L = 2 \times 10^{-7} \times l \times \ln\left(\frac{8A}{lw}\right)$$ Equation 4-6

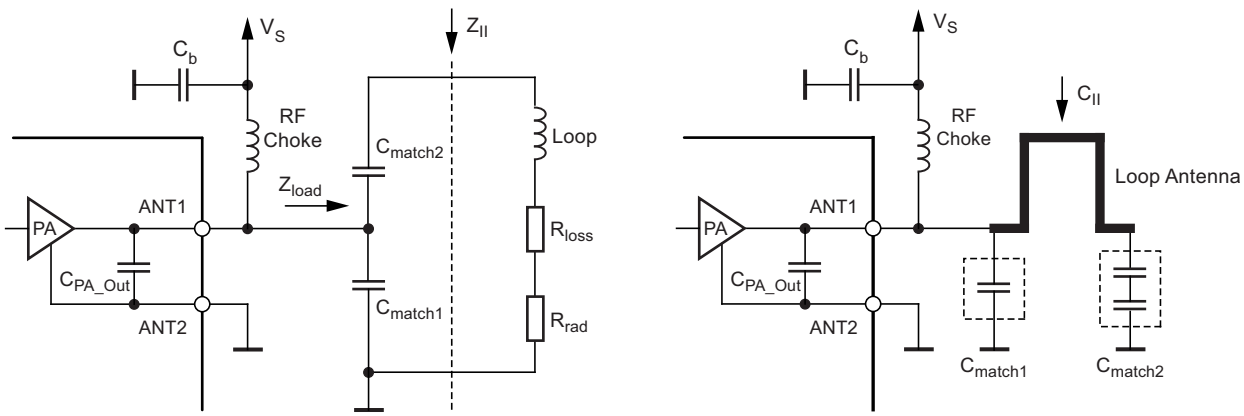
Notes:
1. L = loop perimeter
2. A = loop area
3. W = trace width of the loop antenna

$$Q_{loop} = \frac{\omega L_{loop}}{R_{loss}}$$ Equation 4-7

Figure 2-2a shows the principle of the loop antenna matching to the power amplifier of the ATA5749. The two matching capacitors, C_{match1} and C_{match2}, form the antenna resonance and provide by transformation the optimal load impedance (Z_{LOPT}) required by the power amplifier. To reduce the tolerance influence two serial capacitors can replace C_{match1} and C_{match2}. As mentioned in Section 1.4.2 “Output Matching to 50Ω Load” on page 7 the decoupling capacitor (Cb) is necessary for the PA supply blocking and must be placed as close as possible to both the RF choke and pin ANT1. The recommended capacitor Cb value is 1nF (X7R). The RF choke should provide a low resistive path from the PA's output to VS. Please note that this matching procedure targets to deliver the entire RF current from the PA to the antenna.

The antenna Q-factor must be well chosen to properly handle the tolerances of the elements during the matching progress as well as during mass production later on. The Q-factor should not be too large, and thus the trace width of the printed antenna must be less than 1.5 mm.

Figure 2-2. The Principle Matching of the Loop Antenna to the Power Amplifier



a (with Equivalent Loop Antenna Circuit)

b (Standard Schematic without Equivalent Loop Antenna Circuit

Equations 4-8 to 4-13 help to calculate the start values of the matching elements during the tuning process. The calculation refers to the circuit in Figure 2-2a. First, the parallel resonance impedance ($Z_{||}$) can be calculated by formula 4-8.

$$Z_{||} = Q_{loop} \times 2\pi f L_{loop} \qquad \text{Equation 4-8}$$

$$Z_{II} = r^2 \times Z_{load} \qquad \text{Equation 4-9}$$

Note: r = transformation ratio of the matching structure ($C_{match1,2}$)

$$C_{II} = \frac{1}{\omega^2 L_{loop}} = \frac{(C_{match1} + C_{PA\_Out}) \times C_{match2}}{(C_{match1} + C_{PA\_Out}) + C_{match2}} \qquad \text{Equation 4-10}$$

$$r = \frac{(C_{match1} + C_{PA\_Out}) + C_{match2}}{C_{match2}} \qquad \text{Equation 4-11}$$

The C_{match1} and C_{match2} can be given as,

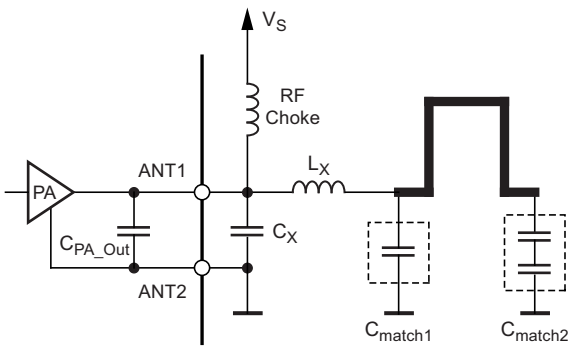
$$C_{match1} = r \times C_{II} - C_{PA\_OUT} \qquad \text{Equation 4-12}$$

$$C_{match2} = \frac{(C_{match1} + C_{PA\_Out})}{r - 1} \qquad \text{Equation 4-13}$$

Caution: The calculated C_{match1} and C_{match2} values are only the theoretical start values for the tuning process.

With regard to the 1st harmonic suppression, Cmatch1 must be placed as close as possible to the power amplifier. If a higher harmonic rejection is needed an additional low-pass filter has to be inserted in the matching circuit. Figure 2-3 shows the principle schematic using an additional low-pass filter to improve the harmonics suppression. The capacitor C_X must be placed as close as possible to the power amplifier output and properly fixed to both pin ANT2 and the ground plate.

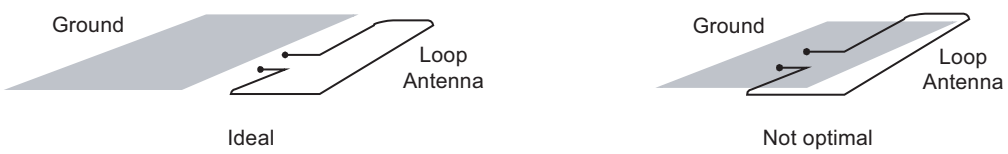
Figure 2-3. Matching Structure of the Loop Antenna with an Additional Low Pass Filter



The following rules must be observed when designing a loop antenna:

- In case of a small loop antenna, the area enclosed by the loop has to be designed as large as possible
- The ground area within the loop must be small
- As the field density increases at the loop edges, sufficient space must be provided near the loop edges

Figure 2-4. Comparison of an Ideal and a Poor Loop Antenna Layout Design



2.3 Application Circuit and Layout Design Hints

The following rules must be adhered to achieve optimum module performance:

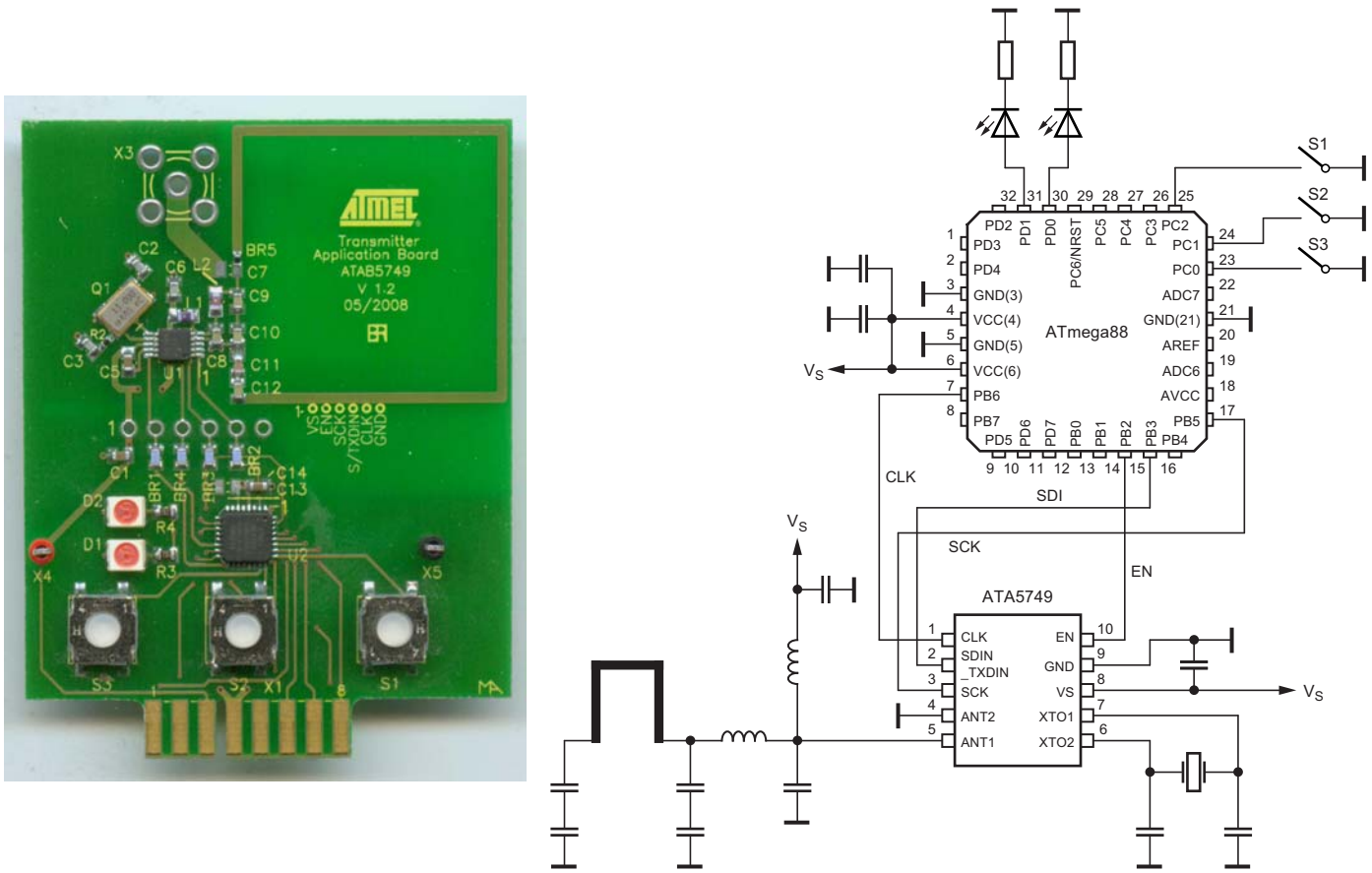
- The connection of pin ANT2 to ground must be designed properly. The best practical way is to place several vias directly to the board's ground plate. This rule is also valid for the ground connection of the matching elements.
- The conductive trace for the clock signal from the ATA5749 to the microprocessor must be designed very carefully and as short as possible.
- Each blocking capacitor (especially the decoupling capacitor for the ATA5749's supply voltage) must be placed as close as possible to the power supply pin to be decoupled. The recommended value for the decoupling capacitor is 68nF (X7R).
- The crystal must be placed as close as possible to the IC.

2.4 Developing an Application-specific ATA5749 Design using Atmel's Demo Boards

For developing purposes, Atmel offers 2 different boards, the demo board ATAB5749-x and ATA5749-EKx. The ATA5749-EKx is a stand-alone board, where the pre-defined board settings can not be changed unless the software is changed. In case the transmitter settings need to be modified, engineers should use the demo board ATAB5749-x (changes of the software, however, can not be done with this board). Certain settings of the ATAB5749-x can be modified using software installed in the Windows® operating system.

2.4.1 Short Information on ATAB5749-x

Figure 2-5. ATAB5749-x: Simplified Schematic and Demo Board Picture



The microprocessor board ATAB-RFMB and the “RF Design Kit Software” are needed to start the verification. The application note “Getting Started with ATAB5749 Using RF Design Kit Software” explains how to operate the demo kit. This document is available online on Atmel’s website at http://www.atmel.com/dyn/resources/prod_documents/doc9138.pdf.

Notes:
1. ATAB5749-3 is matched to 315MHz
2. ATAB5749-4 is matched to 433.92MHz
3. For IC verification:
   - ATAB-RFMB, (including the Software RF Design Kit
   - ATAB5749-3/4

2.4.1.1 Short Description of the Demo Software

The main issue is how to generate an accurate data rate to modulate the transmitter. To this end the ATA5749’s clock signal can be used as an external reference to calibrate the internal RC oscillator. The data rate tolerance of the transmitter module will be much tighter than the tolerance of the internal RC oscillator - even if only one crystal is used for the transmitter and the microprocessor. For this purpose the “external” clock, provided by the ATA5749, must be connected to the microprocessor's timer/counter pin (please refer to Figure 2-5 on page 17).

Touching a button causes the following events:

1. Start of the microprocessor with its internal RC oscillator
2. Configuration of the 32-bit control register via SPI interface
3. Waiting for the clock signal generated by the transmitter
4. Calibration start of the internal RC oscillator once the ATA5749’s clock signal is available
5. Shifting the telegram to ATA5749

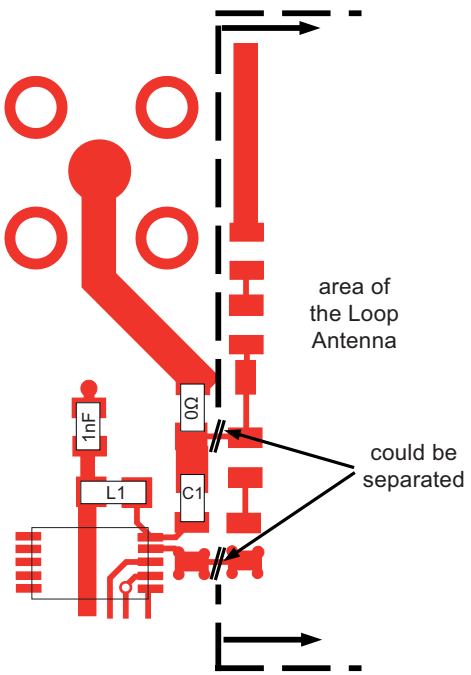
Note: The RC oscillator’s calibration must be performed for each telegram transmission.

To minimize the current consumption on the demo board the ATmega88 always remains in power-down mode until an event occurs. The activation of a button wakes up the microprocessor using a pin change interrupt. To further reduce the current consumption the watchdog timer and brown-out detection are disabled. As the microprocessor’s ADC is not used it is also switched off (please refer to the Power Reduction Register (PRR) of ATmega48/88).

2.4.1.2 Measurement with 50Ω Interface

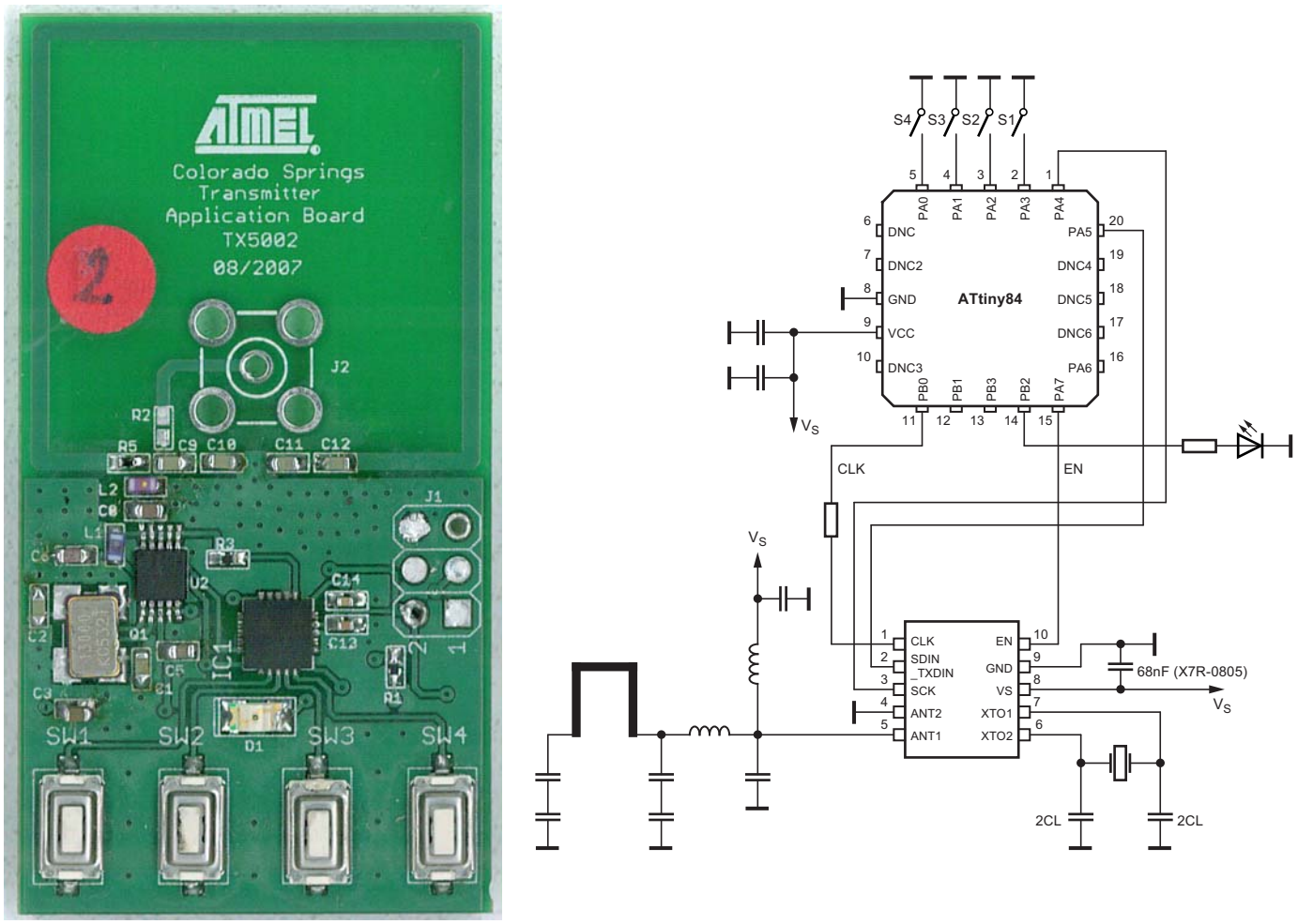
The ATAB5749-x board enables to use an SMB or SMA connector for measurement purposes. Figure 2-6 shows a detail of the board layout with the IC and the 50Ω output. It illustrates how the connector and the matching elements can be mounted. The inductor L1 and capacitor C1 values can be taken from Table 1-1 on page 4 and Table 1-2 on page 4.

Figure 2-6. Section of ATAB5749-x for 50Ω Measurement



2.4.2 Short Information on ATA5749-EKx

Figure 2-7. ATA5749-EKx: Simplified Schematic and Demo Board Picture

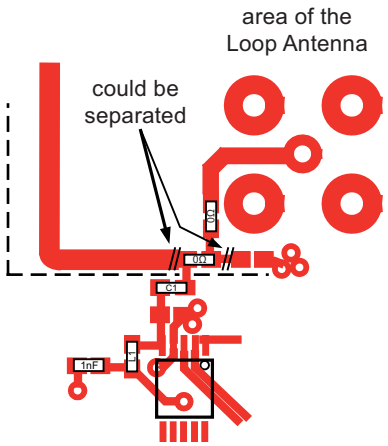


Notes: 1. ATA5749-EK1 is matched to 315MHz
2. ATA5749-EK2 is matched to 433.92MHz

2.4.2.1 Measurement with 50Ω Interface

Same as the ATAB5749-x demo board, the ATA5749-EKx enables to use an SMB or SMA connector for measurement purposes. Figure 2-8 shows a detail of the board layout with the IC and the 50Ω output. It illustrates how the connector and the matching elements can be mounted.

Figure 2-8. Section of ATAB5749-x for 50Ω Measurement



2.4.2.2 Approval Test

The boards ATA5749-EK1 and ATA5749-EK2 were tested by an authorized test house according to the FCC (part 15) and ETSI (EN 300 220-1 V2.1.1) regulations. These tests demonstrate that the ATA5749 on the ATA5749-EKx demo boards is able to achieve the common type approval for automotive applications.

3. ANNEX

Table 3-1. Organization of the 32 Bit Control Register

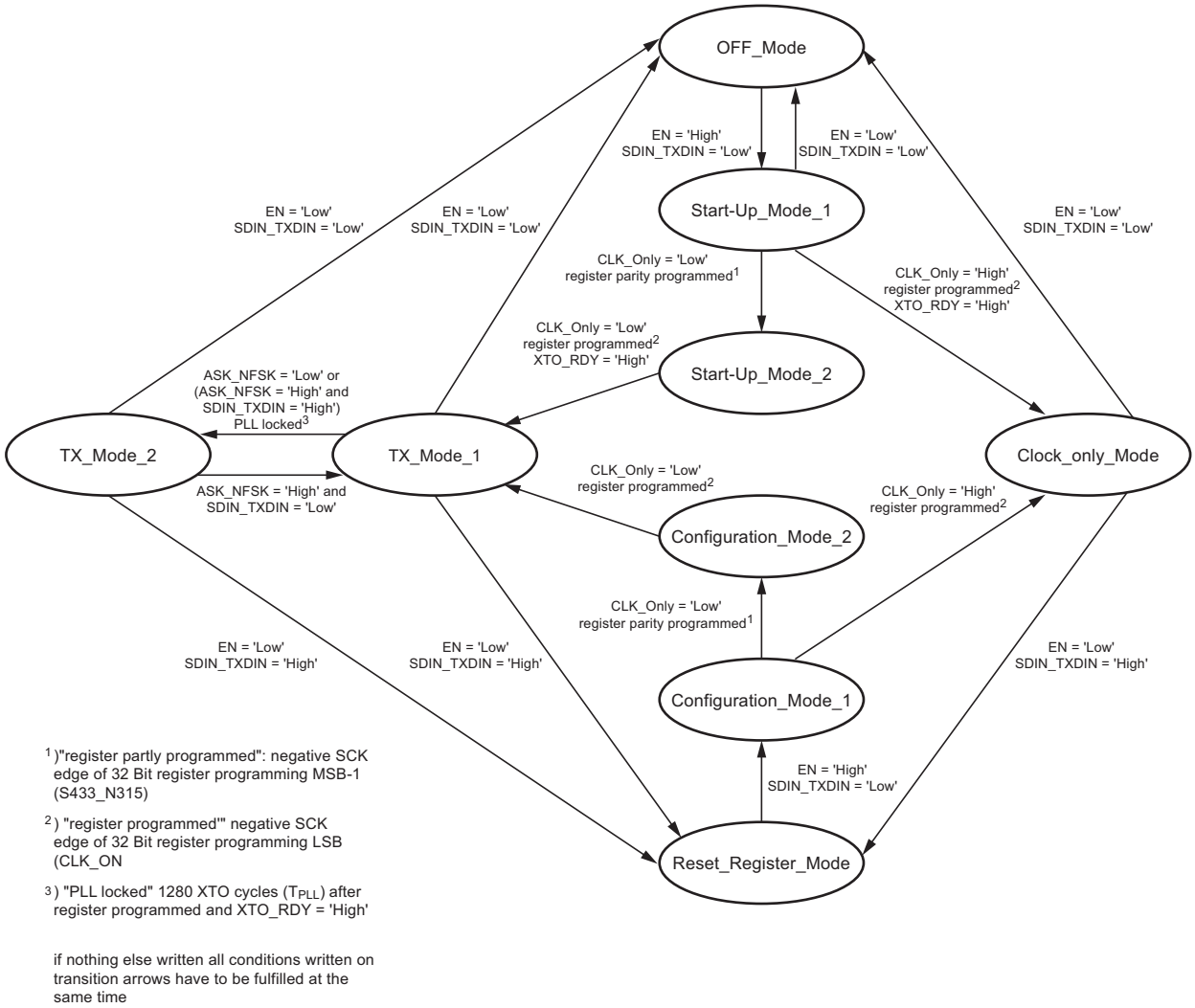
MSB															
31 CLK_ Only	30 S434_ N315	29 FREQ [14]	28 FREQ [13]	27 FREQ [12]	26 FREQ [11]	25 FREQ [10]	24 FREQ [9]	23 FREQ [8]	22 FREQ [7]	21 FREQ [6]	20 FREQ [5]	19 FREQ [4]	18 FREQ [3]	17 FREQ [2]	16 FREQ [1]
		Frequency Adjust FREQ = FREQ[0] + 2 × FREQ[1] + 4 × FREQ[2] + ... + FREQ[14] × 16384 = 0 .. 32767													

															LSB
15 FREQ [0]	14 FSEP [7]	13 FSEP [6]	12 FSEP [5]	11 FSEP [4]	10 FSEP [3]	9 FSEP [2]	8 FSEP [1]	7 FSEP [0]	6 DIV_ CNTRL	5 PWR [3]	4 PWR [2]	3 PWR [1]	2 PWR [0]	1 ASK_ NFSK	0 CLK_ ON
	FSK Shift FSEP = FSEP[0] + ... + FSEP[7] × 128 = 0 .. 255									Output Power PWR = PWR[0] + .. + PWR[3] × 8 = 0.. 15					

Table 3-2. Register Description

Name	Bit Number	Bit Count	Remarks
CLK_Only	31	1	Activates / deactivates CLK_Only Mode CLK_only = “Low” normal Mode CLK_only = ‘”High’” CLK_Only Mode in Figure 1-10 on page 13
S434_N315	30	1	VCO Band Selection and divider control “High”: 367 .. 450MHz “Low”: 300 .. 368MHz
FREQ[0:14]	15 ... 29	15	Values 0 .. 32767 PLL frequency adjust
FSEP[0:7]	7 ... 14	8	Values 0 .. 255 FSK Deviation setting
DIV_CNTRL	6	1	CLK output Divider Ratio “Low”: $f_{CLK} = f_{XTO}/8$ “High”: $f_{CLK} = f_{XTO}/4$
PWR[0:3]	2 ... 5	4	Values 0 .. 15 see Table 1-1 on page 4. PA Output Power Adjustment PWR = 3 .. 15 --> Pout = –0.5dBm .. 12.5dBm in approximately 1 dB steps see Table 1-4 on page 8 and Table 1-5 on page 8
ASK_NFSK	1	1	Modulation Type “Low”: FSK “High”: ASK
CLK_ON	0	1	CLK_DRV port de-/activation “High”: CLK port is ON “Low”: CLK port is OFF

Figure 3-1. Flowchart Operation Modes



1)"register partly programmed": negative SCK edge of 32 Bit register programming MSB-1 (S433_N315)

2) "register programmed"" negative SCK edge of 32 Bit register programming LSB (CLK_ON

3) "PLL locked" 1280 XTO cycles (T_{PLL}) after register programmed and XTO_RDY = 'High'

if nothing else written all conditions written on transition arrows have to be fulfilled at the same time

4. Revision History

Please note that the following page numbers referred to in this section refer to the specific revision mentioned, not to this document.

Revision No.	History
9169C-RKE-05/15	• Put document in the latest template

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