SINGLE SUPPLY SYNCHRONOUS PWM CONTROLLER WITH FIXED 5V OUTPUT AND 3.3V/700mA LDO

Pb Free Product

DESCRIPTION

The NX2837 controller IC is a single power supply synchronous Buck controller IC designed for step down DC to DC converter applications. NX2837 is optimized to convert bus voltages from 9V to 22V to fixed 5V output. This switching 5V output is the input supply of an internal 3.3V LDO which can provide output current up to 700mA. An internal regulator converts bus voltage to 5V, which provides voltage supply to internal logic and driver circuit. The NX2837 operates at 350kHz and employs fixed loss-less current limiting by sensing the Rdson of synchronous MOSFET followed by hiccup feature.Feedback under voltage triggers Hiccup.
Other features of the device are: Internal schottky diode, 3.3V LDO power good indicator, Thermal shutdown, 5V gate drive, Adaptive deadband control, Internal digital soft start, Vcc undervoltage lock out and Shutdown capability via the comp pin.

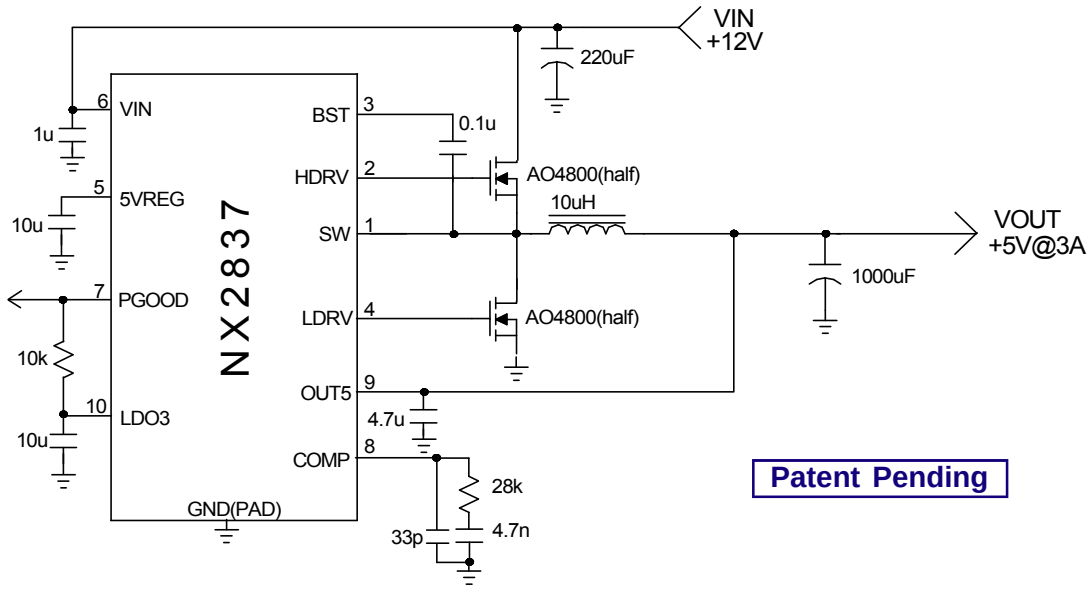
FEATURES

- Single supply voltage from 9V to 22V
- Internal 5V regulator
- Fixed 350kHz working frequency
- Internal Digital Soft Start Function
- Fixed 5V switching output
- Internal 700mA 3.3VLDO with Power Goood indicator
- Prebias Startup
- Less than 50 nS adaptive deadband
- Fixed current limit triggers hiccup by sensing Rdson of Synchronous MOSFET
- Pb-free and RoHS compliant

APPLICATIONS

- LCD TV
- Graphic Card on board converters
- On board DC to DC application
- Hard Disk Drive
- Set Top Box

TYPICAL APPLICATION



Patent Pending

Figure1 - Typical application of 2837

ORDERING INFORMATION

Device	Temperature	Package	Frequency	Pb-Free
NX2837CUPTR	0 to 70°C	MSOP-EP-10L	350kHz	Yes

Package Marking : NX2837XXX XXX is date code.
For example, 735 means that this NX2837 is packaged in the 35th week of 2007

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ABSOLUTE MAXIMUM RATINGS(NOTE1)

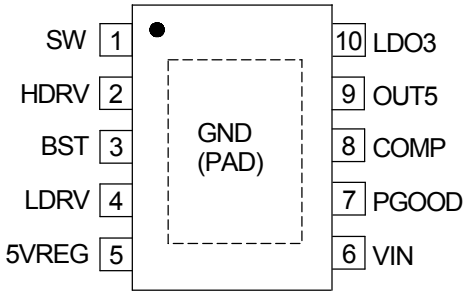
5VREG to GND & BST to SW voltage 6.5V
BST to GND Voltage 30V
VIN to GND Voltage 25V
SW to GND ..... -2V to 30V
All other pins ..... -0.3V to 6.5V
Storage Temperature Range ..... -65°C to 150°C
Operating Junction Temperature Range ..... -40°C to 125°C

NOTE1: Stresses above those listed in "ABSOLUTE MAXIMUM RATINGS", may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

PACKAGE INFORMATION

10-LEAD PLASTIC MSOP-EP

$\theta_{JA} \approx 46^{\circ}C/W$



ELECTRICAL SPECIFICATIONS

Unless otherwise specified, these specifications apply over Vin = 12V, and T_A=0 to 70°C. Followings are bypass capacitors:C_{VIN}=1uF, C_{5VREG}=10uF, C_{LDO3}=10uF, all X5R ceramic capacitors. Typical values refer to T_A = 25°C. Low duty cycle pulse testing is used which keeps junction and case temperatures equal to the ambient temperature.

PARAMETER	SYM	Test Condition	Min	TYP	MAX	Units
OUT5 Voltage						
OUT5 Voltage	V_5		4.75	5	5.24	V
OUT5 Voltage line regulation		V_{IN}=9V to 22V		10	15	mV
5V REG						
5VREG Output			4.8	5	5.4	V
5VREG UVLO		5V REG rising		3.9	4.4	V
5VREG UVLO Hysteresis				0.2		V
5VREG Line Regulation		V_{IN}=9V to 30V		10	30	mV
5VREG Max Current			20	50		mA
Supply Voltage(Vin)						
V_{in} Voltage Range	V_{in}		9		30	V
Input Voltage Current(Static)		No switching	3	3.9	5.3	mA
Input Voltage Current (Dynamic)		Switching with HDRV and LDRV open	3.5	4	6	mA

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PARAMETER	SYM	Test Condition	Min	TYP	MAX	Units
Vin UVLO						
V_{in}-Threshold	V_{in}_UVLO	V_{CC} Rising	6	6.5	7.5	V
V_{in}-Hysteresis	V_{in}_Hyst	V_{CC} Falling		0.6		V
SS						
Soft Start time	Tss		2.4	2.9	3.4	mS
Oscillator (Rt)						
Frequency	F_S		290	350	410	kHz
Ramp-Amplitude Voltage	V_{RAMP}		1.4	1.5	1.9	V
Max Duty Cycle			78	83	90	%
Min Controlable On Time					150	nS
Error Amplifiers						
Transconductance			1500	2000	2500	umho
Comp SD Threshold				0.3		V
OUT5 UVLO						
OUT5 UVLO threshold			2.4	3	3.6	V
High Side Driver(C_L=2200pF)						
Output Impedance , Sourcing	R_{source}(Hdrv)	I=200mA		1.9		ohm
Output Impedance , Sinking	R_{sink}(Hdrv)	I=200mA		1.7		ohm
Rise Time	THdrv(Rise)			14		ns
Fall Time	THdrv(Fall)			17		ns
Deadband Time	Tdead(L to H)	Ldrv going Low to Hdrv going High, 10%-10%		30		ns
Low Side Driver (C_L=2200pF)						
Output Impedance, Sourcing Current	R_{source}(Ldrv)	I=200mA		1.9		ohm
Output Impedance, Sinking Current	R_{sink}(Ldrv)	I=200mA		1		ohm
Rise Time	TLdrv(Rise)			13		ns
Fall Time	TLdrv(Fall)			12		ns
Deadband Time	Tdead(H to L)	SW going Low to Ldrv going High, 10% to 10%		10		ns
LDO						
Output Voltage			3.23	3.3	3.37	V
Line regulation				5	10	mV
Load regulation					2	%
current limit				900		mA
OCP						
OCP threshold			420	480	625	mV
3.3V Power Good						
Threshold Voltage as % of Vref		FB ramping up	85	90	95	%
Hysteresis				5		%
Over temperature						
Threshold				150		°C
Hysteresis				20		°C
Internal Schottky Diode						
Forward voltage drop		forward current=20mA		350	500	mV

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PIN DESCRIPTIONS

PIN #	PIN SYMBOL	PIN DESCRIPTION
5	5VREG	An internal 5V regulator provides supply voltage for the low side fet driver, BST and internal logic circuit. A high frequency 10uF ceramic capacitor must be connected from this pin to the GND pin as close as possible
6	VIN	Voltage supply for the internal 5V regulator. A high freuqncy 1uF ceramic capacitor must be connected from this pin to GND.
9	OUT5	This pin is used to sense the output voltage of converter and regulates the output voltage to 5V. This pin is connected to the output UVLO comparator. When this pin falls below 3V, both HDRV and LDRV outputs are in hiccup.This pin also is the input of internal 3.3V LDO.
8	COMP	This pin is the output of the error amplifier and is used to compensate the voltage control feedback loop. This pin is also used as a shut down pin. When this pin is pulled below 0.3V, both drivers are turned off and internal soft start is reset.
3	BST	This pin supplies voltage to the high side driver. A high frequency ceramic capacitor of 0.1 to 1 uF must be connected from this pin to SW pin.
10	LDO3	This pin is the output of internal 3.3V LDO. A minimum of 10uF/X5R capacitor must be connected from this pin to ground to ensure stability.
1	SW	This pin is connected to the source of the high side MOSFET and provides return path for the high side driver.
2	HDRV	High side MOSFET gate driver.
PAD	GND	Ground pin.
4	LDRV	Low side MOSFET gate driver.
7	PGOOD	An open drain output that requires a pull up resistor to LDO3 or Vcc. When LDO3 reaches 90% of 3.3V, PGOOD transitions from LO to HI state.

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BLOCK DIAGRAM

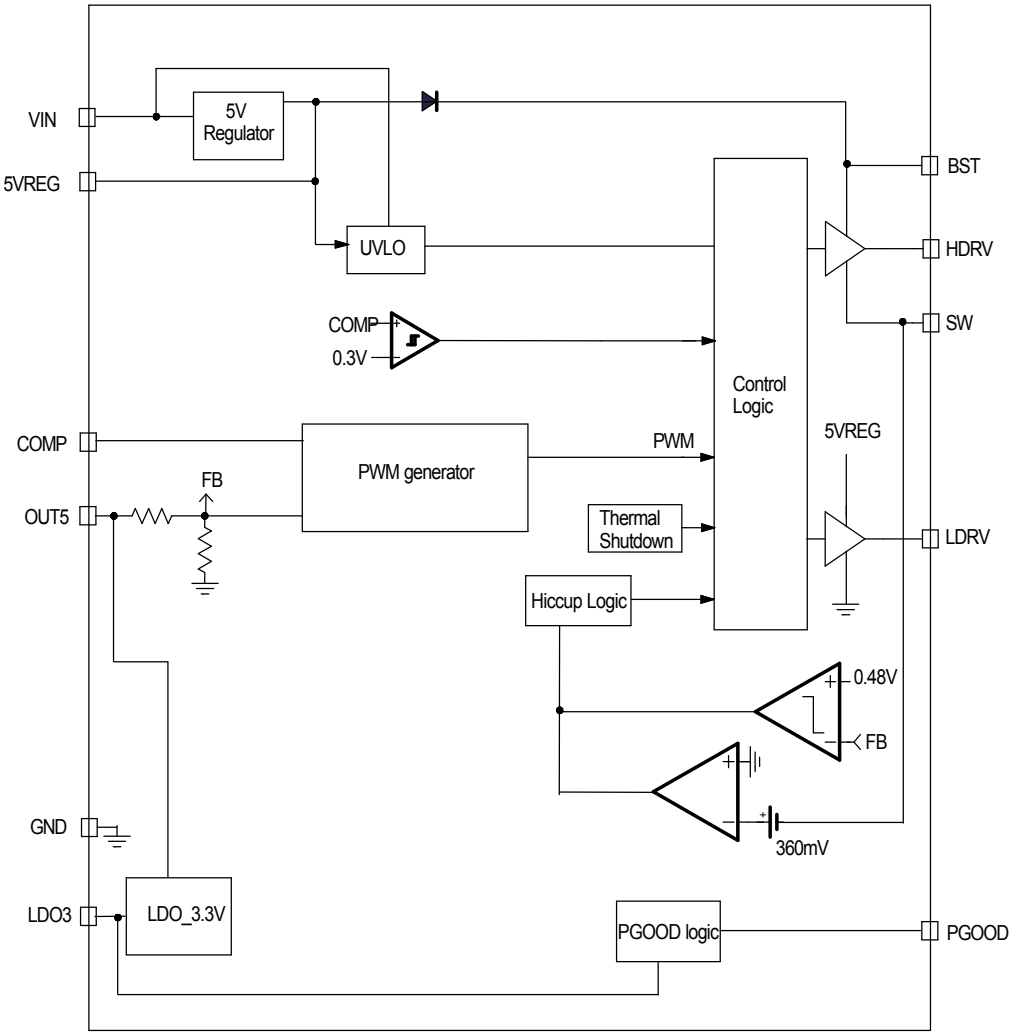

Figure 2 - Simplified block diagram of the NX2837

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Demoboard Design

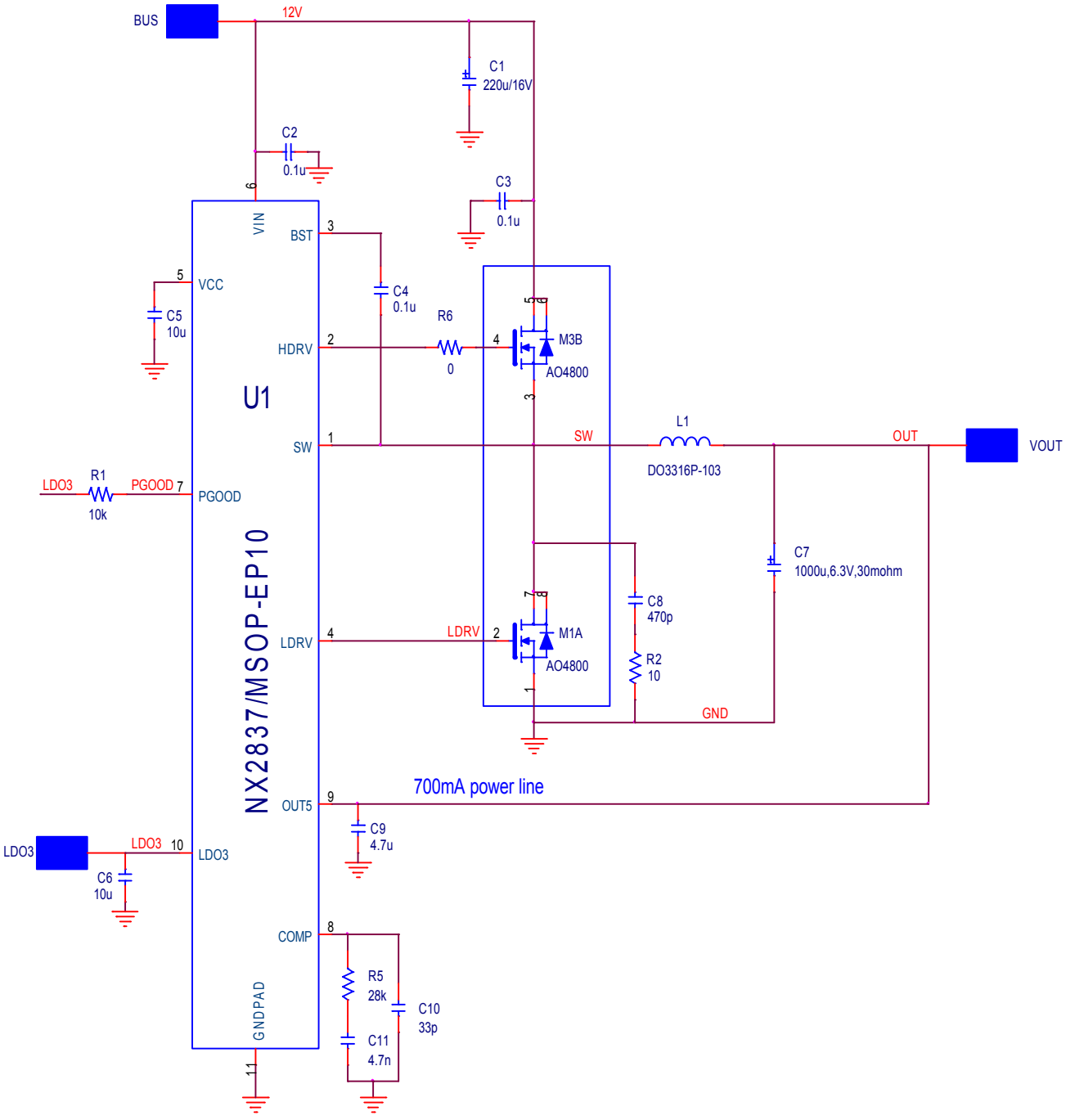

Figure 3 - demoboard schematic of NX2837

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Bill of Materials

Item	Quantity	Reference	Part
1	1	C1	220u/16V/ELEC
2	3	C2,C3,C4	0.1u
3	2	C5,C6	10u,6.3V,X5R
4	1	C7	1000u,6.3V,30mohm
5	1	C8	470p
6	1	C9	4.7u,6.3V,X5R
7	1	C10	33p
8	1	C11	4.7n
9	1	L1	DO3316P-103
10	1	M2	AO4800
11	1	R1	10k
12	1	R2	10
13	1	R5	28k
14	1	R6	0
15	1	U1	NX2837/MSOP-EP10

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Demoboard Waveforms

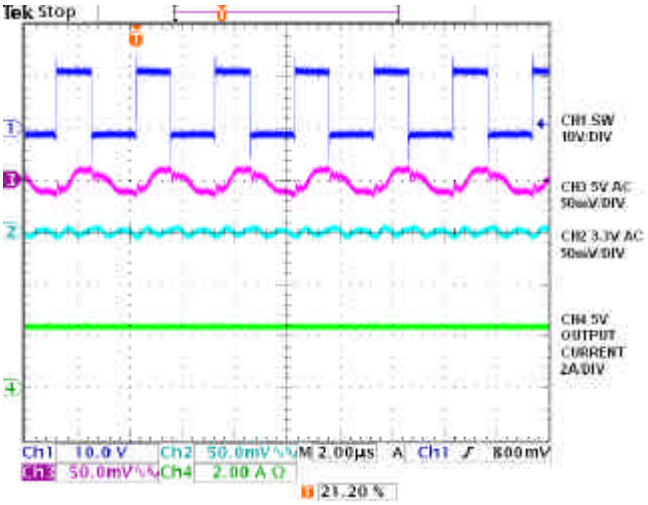

Fig.4 Output ripple(5V@2A,3,3V@650mA)

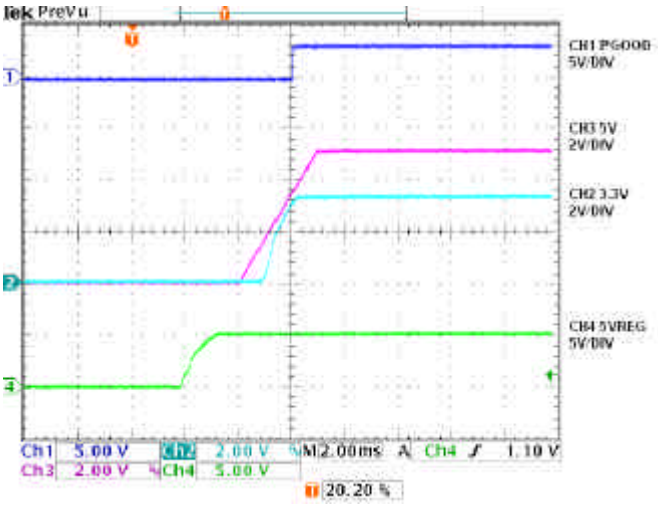

Fig.5 Startup

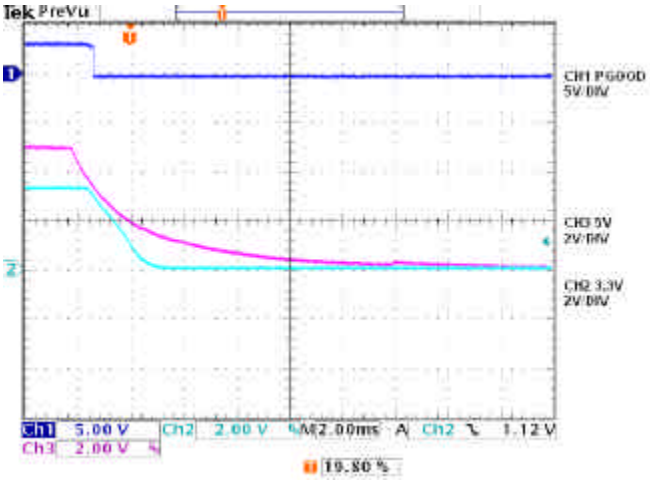

Fig.6 Shutdown

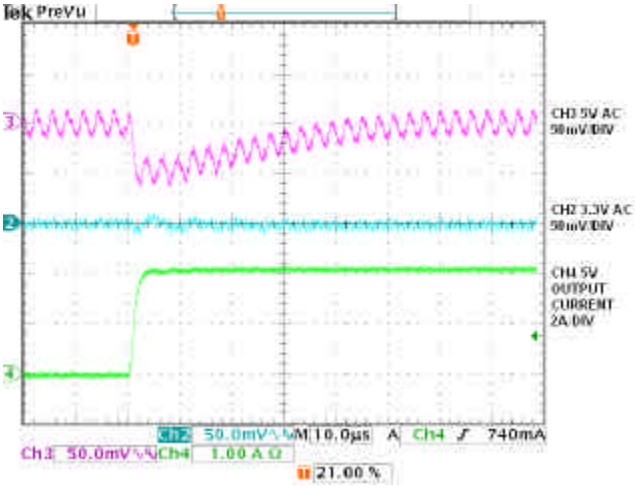

Fig.7 5V step response(5V@2A step, 3.3V@600mA DC)

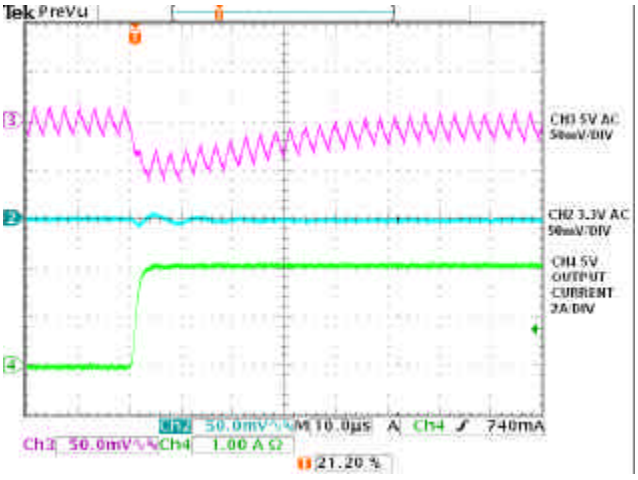

Fig.8 step dynamic response(3.3V@no load)

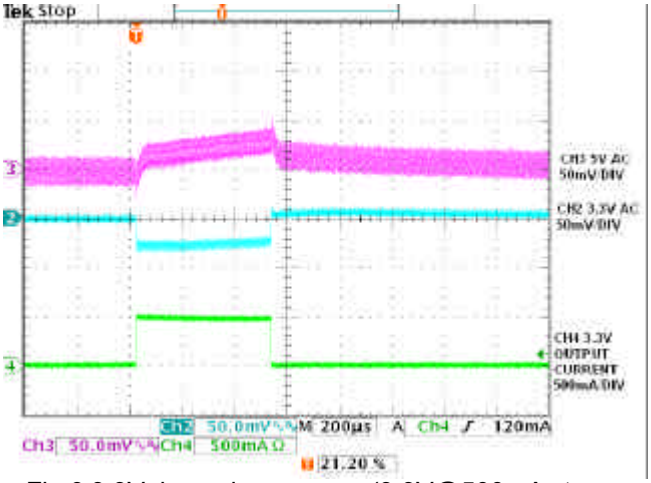

Fig.9 3.3V dynamic response (3.3V@500mA step, 5V@1A DC)

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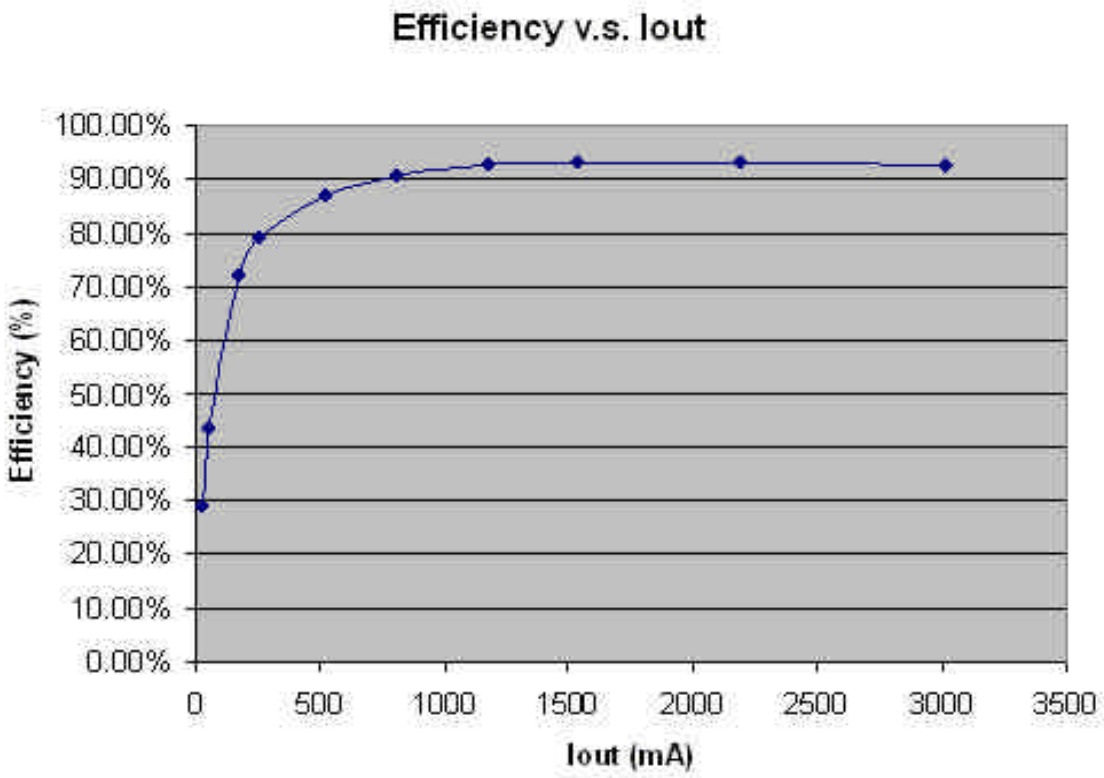

Fig.10 Output efficiency(VIN=12V, VOUT=5V)

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APPLICATION INFORMATION

Symbol Used In Application Information:

V_{IN} - Input voltage
V_{OUT} - Output voltage
I_{OUT} - Output current
ΔV_{RIPPLE} - Output voltage ripple
F_S - Working frequency
ΔI_{RIPPLE} - Inductor current ripple

Design Example

The following is typical application for NX2837, the schematic is figure 1.

V_{IN} = 12V
V_{OUT}=5V
F_S=350kHz
I_{OUT}=3A
ΔV_{RIPPLE} <=50mV
ΔV_{DROOP}<=250mV @ 1A step

Output Inductor Selection

The selection of inductor value is based on inductor ripple current, power rating, working frequency and efficiency. Larger inductor value normally means smaller ripple current. However if the inductance is chosen too large, it brings slow response and lower efficiency. Usually the ripple current ranges from 20% to 40% of the output current. This is a design freedom which can be decided by design engineer according to various application requirements. The inductor value can be calculated by using the following equations:

$$L_{OUT} = \frac{V_{INMAX}-V_{OUT}}{\Delta I_{RIPPLE}} \times \frac{V_{OUT}}{V_{INMAX}} \times \frac{1}{F_S} \quad ...(1)$$

$$I_{RIPPLE} = k \times I_{OUTPUT}$$

where k is between 0.2 to 0.4.
Select k=0.3, then

$$L_{OUT} = \frac{12V-5V}{0.3 \times 3A} \times \frac{5V}{12V} \times \frac{1}{350kHz}$$

L_{OUT} =9.2uH

Choose inductor from COILCRAFT DO5022P-103 with L=10uH is a good choice.

Current Ripple is recalculated as

$$\Delta I_{RIPPLE} = \frac{V_{IN}-V_{OUT}}{L_{OUT}} \times \frac{V_{OUT}}{V_{IN}} \times \frac{1}{F_S} = \frac{12V-5V}{10uH} \times \frac{5V}{12V} \times \frac{1}{350kHz} = 0.833A \quad ...(2)$$

Output Capacitor Selection

Output capacitor is basically decided by the amount of the output voltage ripple allowed during steady state(DC) load condition as well as specification for the load transient. The optimum design may require a couple of iterations to satisfy both condition.

Based on DC Load Condition

The amount of voltage ripple during the DC load condition is determined by equation(3).

$$\Delta V_{RIPPLE} = ESR \times \Delta I_{RIPPLE} + \frac{\Delta I_{RIPPLE}}{8 \times F_S \times C_{OUT}} \quad ...(3)$$

Where ESR is the output capacitors' equivalent series resistance,C_{OUT} is the value of output capacitors.

Typically when large value capacitors are selected such as Aluminum Electrolytic,POSCAP and OSCON types are used, the amount of the output voltage ripple is dominated by the first term in equation(3) and the second term can be neglected.

For this example, electrolytic capacitor is chosen as output capacitor, the ESR and inductor current typically determines the output voltage ripple.

$$ESR_{desire} = \frac{\Delta V_{RIPPLE}}{\Delta I_{RIPPLE}} = \frac{50mV}{0.833A} = 60m\Omega \quad ...(4)$$

If low ESR is required, for most applications, multiple capacitors in parallel are better than a big capacitor. For example, for 50mV output ripple, electrolytic capacitor 1000uF with 30mΩ are chosen.

$$N = \frac{ESR_E \times \Delta I_{RIPPLE}}{\Delta V_{RIPPLE}} \quad ...(5)$$

Number of Capacitor is calculated as

$$N = \frac{30m\Omega \times 0.833A}{50mV}$$

N =0.5

The number of capacitor has to be round up to an integer. Choose N =1.

Based On Transient Requirement

Typically, the output voltage droop during transient is specified as:

$\Delta V_{DROOP} < \Delta V_{TRAN}$ @ step load ΔI_{STEP}

During the transient, the voltage droop during the transient is composed of two sections. One Section is dependent on the ESR of capacitor, the other section is a function of the inductor, output capacitance as well as input, output voltage. For example, for the overshoot, when load from high load to light load with a ΔI_{STEP} transient load, if assuming the bandwidth of system is high enough, the overshoot can be estimated as the following equation.

$$\Delta V_{overshoot} = ESR \times \Delta I_{step} + \frac{V_{OUT}}{2 \times L \times C_{OUT}} \times \tau^2 \quad ...(6)$$

where t is the a function of capacitor, etc.

$$\tau = \begin{cases} 0 & \text{if} \quad L \le L_{crit} \\ \dfrac{L \times \Delta I_{step}}{V_{OUT}} - ESR \times C_{OUT} & \text{if} \quad L \ge L_{crit} \end{cases} \quad ...(7)$$

where

$$L_{crit} = \frac{ESR \times C_{OUT} \times V_{OUT}}{\Delta I_{step}} = \frac{ESR_E \times C_E \times V_{OUT}}{\Delta I_{step}} \quad ...(8)$$

where ESR_E and C_E represents ESR and capacitance of each capacitor if multiple capacitors are used in parallel.

The above equation shows that if the selected output inductor is smaller than the critical inductance, the voltage droop or overshoot is only dependent on the ESR of output capacitor. For low frequency capacitor such as electrolytic capacitor, the product of ESR and capacitance is high and $L \le L_{crit}$ is true. In that case, the transient spec is dependent on the ESR of capacitor.

In most cases, the output capacitors are multiple capacitors in parallel. The number of capacitors can be calculated by the following

$$N = \frac{ESR_E \times \Delta I_{step}}{\Delta V_{tran}} + \frac{V_{OUT}}{2 \times L \times C_E \times \Delta V_{tran}} \times \tau^2 \quad ...(9)$$

where

$$\tau = \begin{cases} 0 & \text{if} \quad L \le L_{crit} \\ \dfrac{L \times \Delta I_{step}}{V_{OUT}} - ESR_E \times C_E & \text{if} \quad L \ge L_{crit} \end{cases} \quad ...(10)$$

For example, assume voltage droop during transient is 250mV for 1A load step.

If the electrolytic capacitor 1000uF with 30mΩ is used, the critical inductance is given as

$$L_{crit} = \frac{ESR_E \times C_E \times V_{OUT}}{\Delta I_{step}} = \frac{30m\Omega \times 1000\mu F \times 5V}{1A} = 200\mu H$$

The selected inductor is 10uH which is much smaller than critical inductance. In that case, the output voltage transient is only dependent on the ESR.

number of capacitors is

$$N = \frac{ESR_E \times \Delta I_{step}}{\Delta V_{tran}} = \frac{30m\Omega \times 1A}{200mV} = 0.15$$

The number of capacitors has to satisfied both ripple and transient requirement. Overall, we can choose N=1.

It should be considered that the proposed equation is based on ideal case, in reality, the droop or overshoot is typically more than the calculation. The equation gives a good start. For more margin, more capacitors have to be chosen after the test. Typically, for high frequency capacitor such as high quality POSCAP especially ceramic capacitor, 20% to 100% (for ceramic) more capacitors have to be chosen since the ESR of capacitors is so low that the PCB parasitic can affect the results tremendously. More capacitors have to be selected to compensate these parasitic parameters.

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Compensator Design

Due to the double pole generated by LC filter of the power stage, the power system has 180° phase shift , and therefore, is unstable by itself. In order to achieve accurate output voltage and fast transient response,compensator is employed to provide highest possible bandwidth and enough phase margin.Ideally,the Bode plot of the closed loop system has crossover frequency between1/10 and 1/5 of the switching frequency, phase margin greater than 50° and the gain crossing 0dB with -20dB/decade. Power stage output capacitors usually decide the compensator type. Electrolytic capacitors are typically chosen as NX2837's output capacitors, type II compensator can be used to compensate the system, because the zero caused by output capacitor ESR is lower than crossover frequency.

Type II compensator can be realized by simple RC circuit without feedback as shown in figure 12. R_3 and C_1 introduce a zero to cancel the double pole effect. C_2 introduces a pole to suppress the switching noise. The following equations show the compensator pole zero location and constant gain.

$$Gain = g_m \times \frac{R_1}{R_1 + R_2} \times R_3 \quad \text{... (11)}$$

$$F_z = \frac{1}{2 \times \pi \times R_3 \times C_1} \quad \text{... (12)}$$

$$F_p \approx \frac{1}{2 \times \pi \times R_3 \times C_2} \quad \text{... (13)}$$

For this type of compensator, F_O has to satisfy $F_{LC} < F_{ESR} << F_O <= 1/10 \sim 1/5 F_s$.

The following is parameters for type II compensator design. Input voltage is 30V, output voltage is 5V, output inductor is 10uH, output capacitor is one 1000uF with 30mΩ electrolytic capacitor.

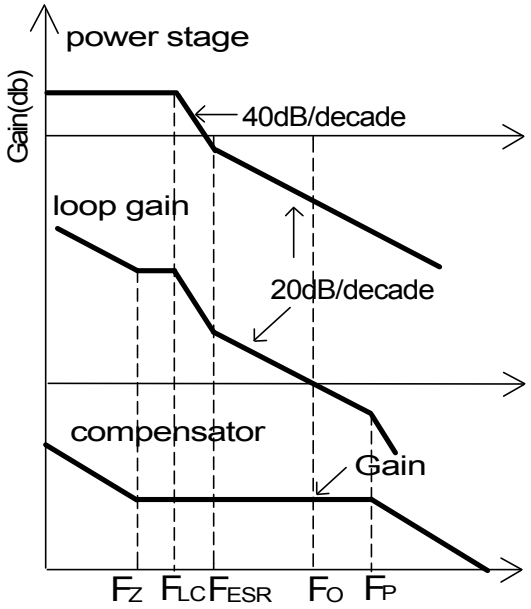

Figure 11 - Bode plot of Type II compensator

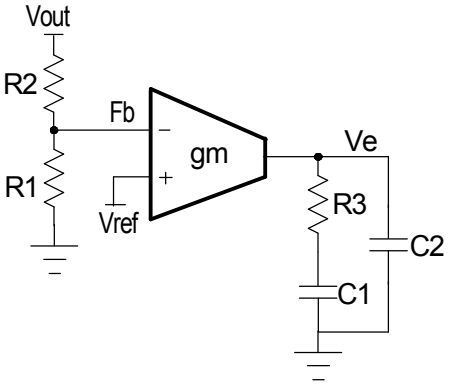

Figure 12 - Type II compensator with transconductance amplifier

1.Calculate the location of LC double pole F_{LC} and ESR zero F_{ESR}.

$$F_{LC} = \frac{1}{2 \times \pi \times \sqrt{L_{OUT} \times C_{OUT}}}$$

$$= \frac{1}{2 \times \pi \times \sqrt{10uH \times 1000uF}}$$

$$= 1.6kHz$$

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$$F_{ESR} = \frac{1}{2\times\pi\times ESR\times C_{OUT}}$$
$$= \frac{1}{2\times\pi\times 30m\Omega\times 1000uF}$$
$$= 5.3kHz$$

2.R_1 and R_2 are internally set to have fixed 5V output. The value of R_1 is 0.8kΩ, and the value of R_2 is 4.2kΩ.

3. Set crossover frequency at 1/10~ 1/5 of the swithing frequency, here F_O=35kHz.

4.Calculate R_3 value by the following equation.

$$R_3 = \frac{V_{OSC}}{V_{in}}\times\frac{2\times\pi\times F_O\times L}{R_{ESR}}\times\frac{1}{g_m}\times\frac{V_{OUT}}{V_{REF}}$$
$$= \frac{1.5V}{12V}\times\frac{2\times\pi\times 35kHz\times 10uH}{30m\Omega}\times\frac{1}{2.0mA/V}\times\frac{5V}{0.8V}$$
$$= 28.6k\Omega$$

Choose R_3 =28kΩ.

5. Calculate C_1 by setting compensator zero F_Z at 75% of the LC double pole.

$$C_1 = \frac{1}{2\times\pi\times R_3\times F_z}$$
$$= \frac{1}{2\times\pi\times 28k\Omega\times 0.75\times 1.6kHz}$$
$$= 4.76nF$$

Choose C_1=4.7nF.

6. Calculate C_2 by setting compensator pole F_p at half the swithing frequency.

$$C_2 = \frac{1}{\pi\times R_3\times F_s}$$
$$= \frac{1}{p\times 28k\Omega\times 350kHz}$$
$$= 32.5pF$$

Choose C_1=33pF.

Input Capacitor Selection

Input capacitors are usually a mix of high frequency ceramic capacitors and bulk capacitors. Ceramic capacitors bypass the high frequency noise, and bulk capacitors supply switching current to the MOSFETs. Usually 1uF ceramic capacitor is chosen to decouple the high frequency noise.The bulk input capacitors are decided by voltage rating and RMS current rating. The RMS current in the input capacitors can be calculated as:

$$I_{RMS} = I_{OUT}\times\sqrt{D}\times\sqrt{1-D}$$
$$D = \frac{V_{OUT}}{V_{IN}} \qquad ...(14)$$

V_{IN} = 12V, V_{OUT}=5V, I_{OUT}=3A, using equation (14), the result of input RMS current is 1.48A.

For higher efficiency, low ESR capacitors are recommended. One Sanyo electrolytic capacitor 35ME470WX(35V 470uF) with 1.8A RMS rating are chosen as input bulk capacitors.

Power MOSFETs Selection

The power stage requires two N-Channel power MOSFETs. The selection of MOSFETs is based on maximum drain source voltage, gate source voltage, maximum current rating, MOSFET on resistance and power dissipation. The main consideration is the power loss contribution of MOSFETs to the overall converter efficiency. In this design example, two AO4800 are used. They have the following parameters: V_{DS}=30V, I_D =6.9A,R_{DSON}=32mΩ,Q_{GATE} =12nC.

There are two factors causing the MOSFET power loss:conduction loss, switching loss.

Conduction loss is simply defined as:

$$P_{HCON} = I_{OUT}^2\times D\times R_{DS(ON)}\times K$$
$$P_{LCON} = I_{OUT}^2\times(1-D)\times R_{DS(ON)}\times K \qquad ...(15)$$
$$P_{TOTAL} = P_{HCON} + P_{LCON}$$

where the $R_{DS(ON)}$ will increases as MOSFET junction temperature increases, K is $R_{DS(ON)}$ temperature dependency. As a result, $R_{DS(ON)}$ should be selected for the worst case, in which K approximately equals to 1.4 at 125°C according to AO4840 datasheet. Conduction loss should not exceed package rating or overall system thermal budget.

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Switching loss is mainly caused by crossover conduction at the switching transition. The total switching loss can be approximated.

$$P_{SW} = \frac{1}{2} \times V_{IN} \times I_{OUT} \times T_{SW} \times F_S \quad ...(16)$$

where I_{OUT} is output current, T_{SW} is the sum of T_R and T_F which can be found in mosfet datasheet, and F_S is switching frequency. Switching loss P_{SW} is frequency dependent.

Also MOSFET gate driver loss should be considered when choosing the proper power MOSFET. MOSFET gate driver loss is the loss generated by discharging the gate capacitor and is dissipated in driver circuits.It is proportional to frequency and is defined as:

$$P_{gate} = (Q_{HGATE} \times V_{HGS} + Q_{LGATE} \times V_{LGS}) \times F_S \quad ...(17)$$

where Q_{HGATE} is the high side MOSFETs gate charge,Q_{LGATE} is the low side MOSFETs gate charge,V_{HGS} is the high side gate source voltage, and V_{LGS} is the low side gate source voltage.

This power dissipation should not exceed maximum power dissipation of the driver device.

Over Current Limit Protection

Over current Limit for step down converter is achieved by sensing current through the low side MOSFET. For NX2837, the current limit is decided by the R_{DSON} of the low side mosfet. When synchronous FET is on, and the voltage on SW pin is below 360mV, the over current occurs. The over current limit can be calculated by the following equation.

$$I_{SET} = 360mV / R_{DSON}$$

The MOSFET R_{DSON} is calculated in the worst case situation, then the current limit for MOSFET AO4800 is

$$I_{SET} = \frac{360mV}{R_{DSON}} = \frac{360mV}{1.5 \times 32m\Omega} = 7.5A$$

Layout Considerations

In high power switching regulator , special attention to the layout must be made in order for the regulate to operate properly and minimize the generated EMI in the system. Since high current is circulated in external power components, the first step is to layout these components such that the trace length is minimized to reduce resistance and even more importantly the trace inductance. In the synchronous buck converter these components are the Input cap, MOSFETs, output inductor and output capacitor. At the same time position the IC such that the upper gate drive and lower gate drive can be connected to the respective gates of the MOSFET with a short and low inductance trace. Next step is to place the most critical components of the IC such as bypass capacitors close to the IC pins as possible. Following is an example of a board layout and a summary of the steps;

1- Place the high frequency ceramic input cap and the bulk cap as close to the drain of the upper MOSFET as possible. Use a plain connection for this trace and also make sure that the drain of the lower MOSFET can be connected to the source of the Upper MOSFET using a short plane connection. Extend the plane connection to output inductor and place the output cap accordingly. Use plane connection here as well. The snubber components, R2 and C8 needs to be connected directly from conjunction of the Drain/Source point to the power GND layer.

2- Place the upper gate resistor and connect the traces using a short trace.

3- Place the BST cap(C4) , Vcc cap(C5), High Frequency input and output caps of the 3.3V LDO, C9 and C6 and Vin cap C2 as close to the IC pins as possible. Make sure that the trace from 5V output of the switching regulator to pin 9 of the IC can handle at least 700mA of average current. Make this trace as wide as possible. Next place the compensation component as close to pin 8 as possible. Place the high frequency cap, C10 first.

Figure 13 to 17 show an example of a circuit layout using a dual Nch MOSFET in sot 23 6L package for reference.

EMI Considerations

Although EMI is related to many factors in switching regulators, however most of the EMI is generated via the power circuitry and proper layout as shown the figure 14 to 17 is a good place to start minimizing it. Both conducted and radiated EMI can be reduced at the expense

of slower rise time of the Upper MOSFET. Although this will come at the expense of higher switching losses, however this option is open to the designer by optimizing the upper gate driver resistance. Another design technique is to place a snubber circuit(C8 and R2) connected directly from the drain of lower MOSFET to GND to eliminate the ringing associated with the parasitic inductance of upper MOSFET source and the drain to source capacitance of the lower MOSFET.

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Appplication Circuit and Demo Board Layout

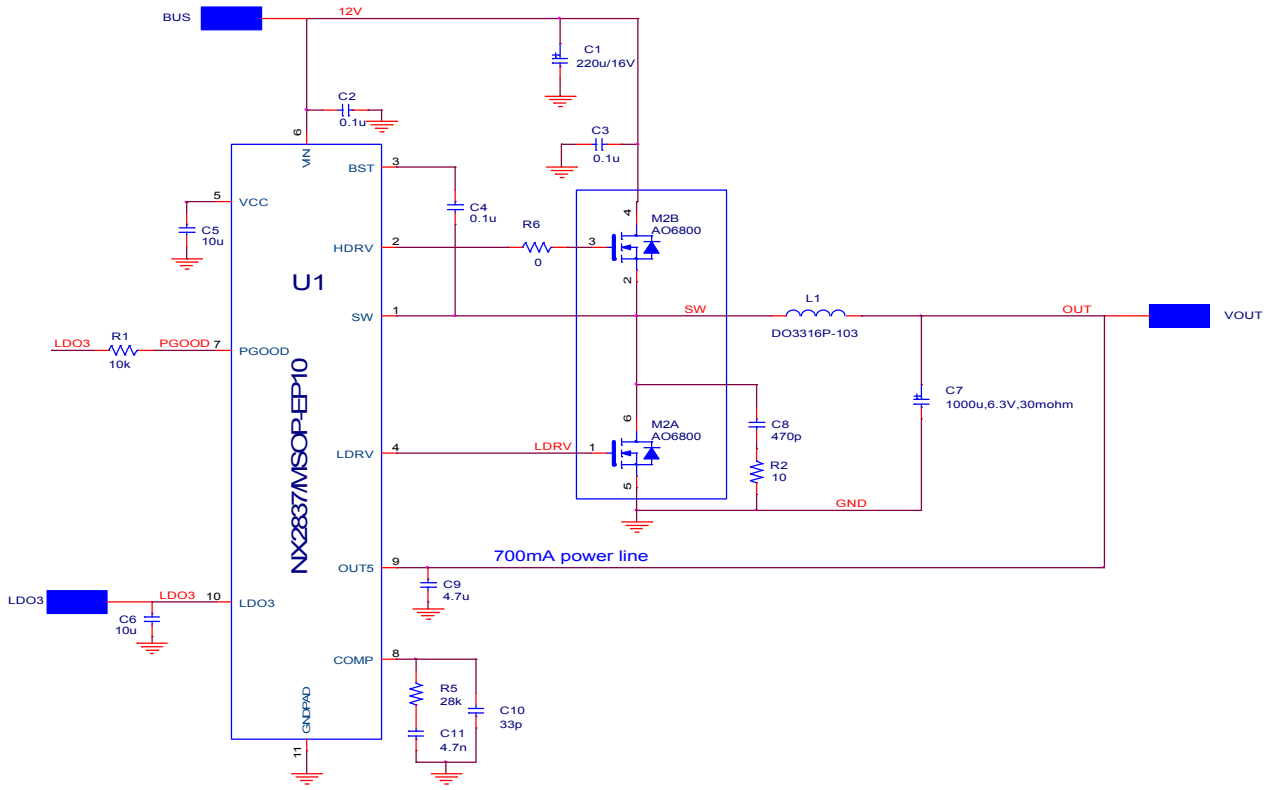

Figure 13 Schematic of application circuit

Bill of Materials

Item	Quantity	Reference	Part
1	1	C1	220u/16V/ELEC
2	3	C2,C3,C4	0.1u
3	2	C5,C6	10u,6.3V,X5R
4	1	C7	1000u,6.3V,30mohm
5	1	C8	470p
6	1	C9	4.7u,6.3V,X5R
7	1	C10	33p
8	1	C11	4.7n
9	1	L1	DO3316P-103
10	1	M2	AO6800
11	1	R1	10k
12	1	R2	10
13	1	R5	28k
14	1	R6	0
15	1	U1	NX2837/MSOP-EP10

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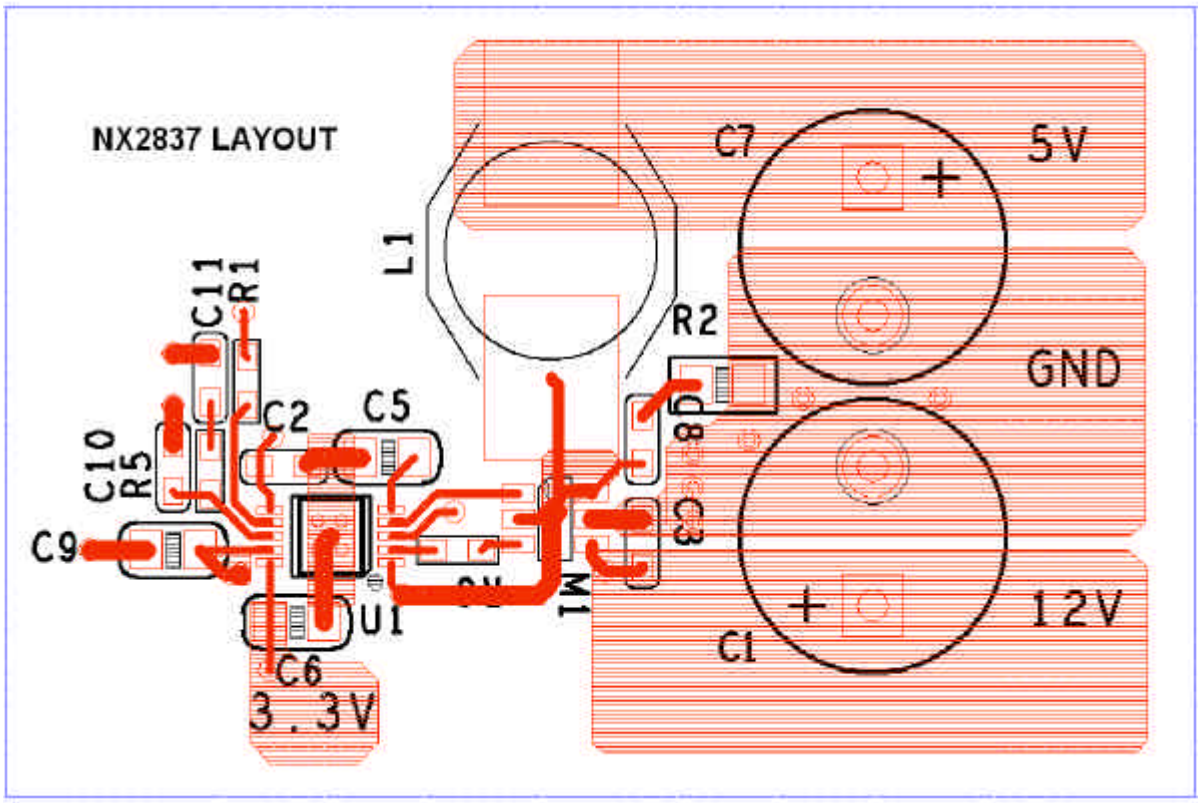

Figure 14 Top layer

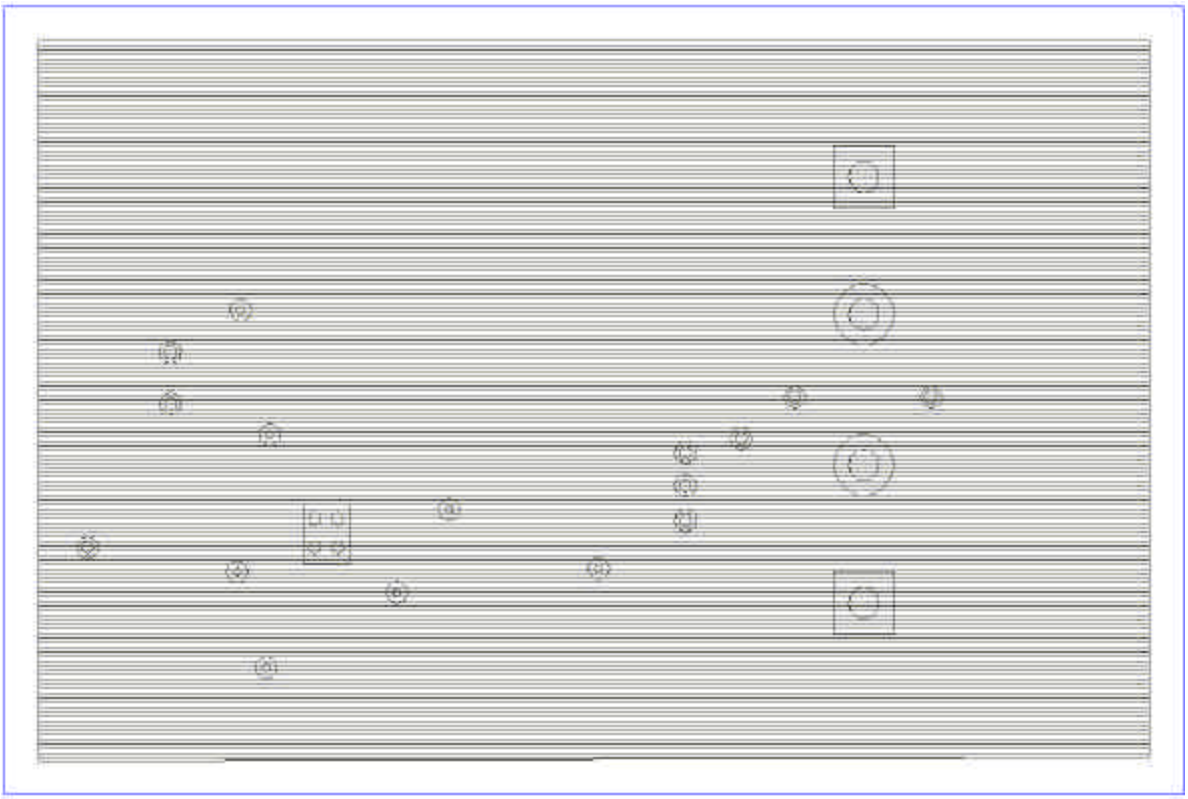

Figure 15 Ground layer

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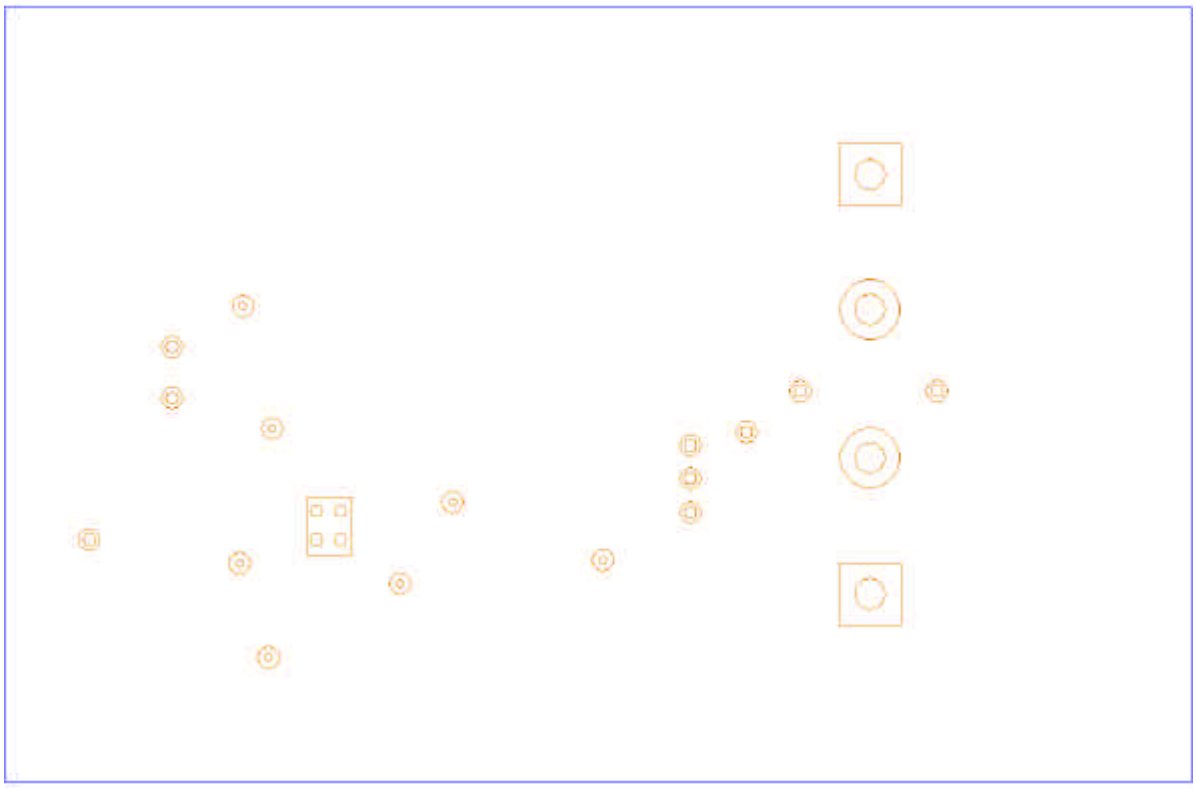

Figure 16 Power layer

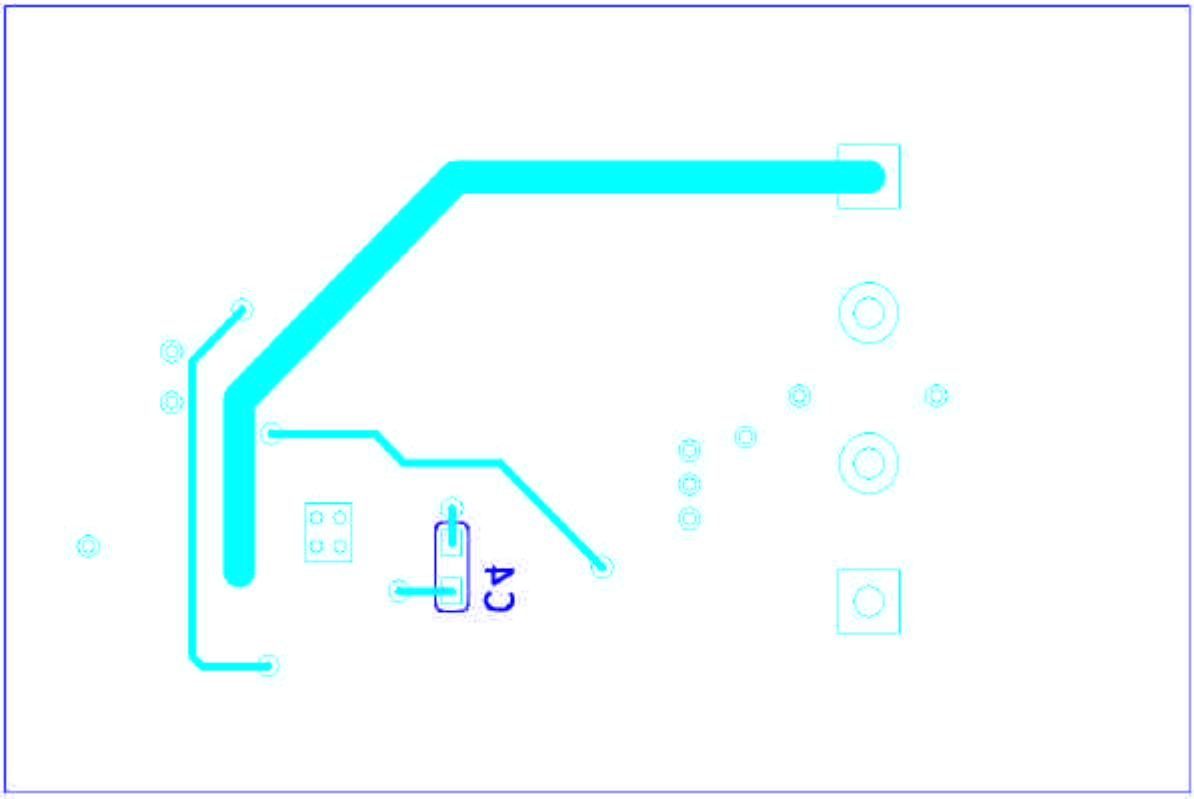

Figure 17 Bottom layer

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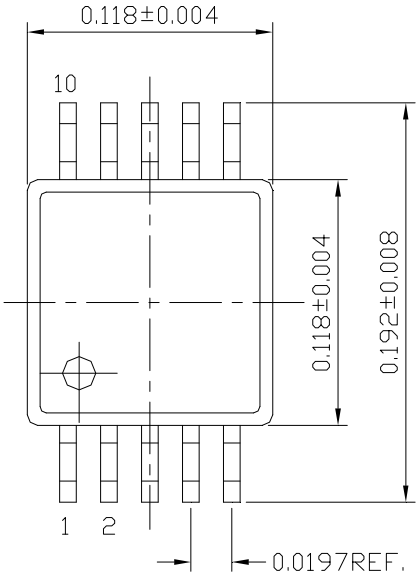
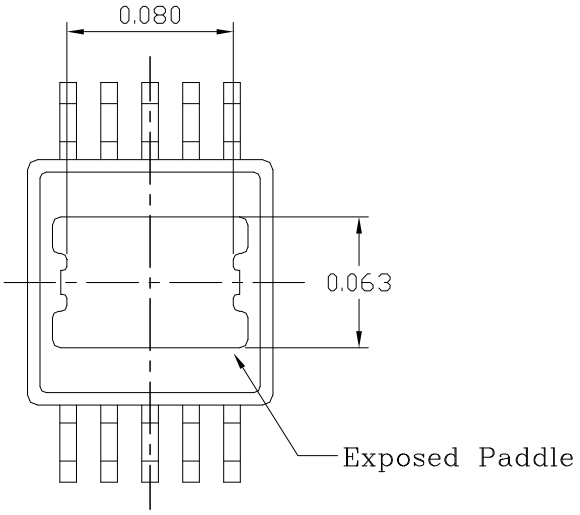
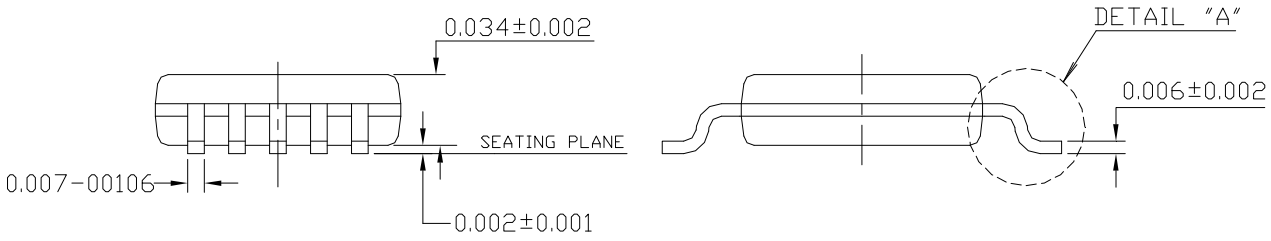
MSOP 10 PIN WITH EXPOSED PAD OUTLINE DIMENSIONS



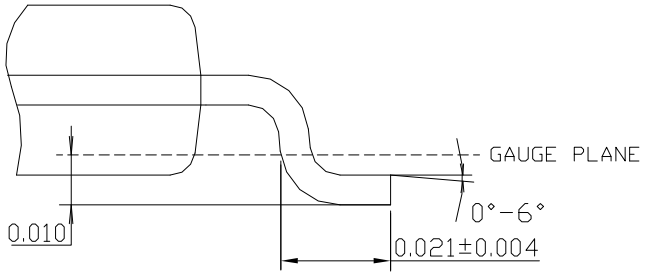
Top View



Bottom View



Side View



DETAIL "A"

NOTE: ALL DIMENSIONS ARE DISPLAYED IN INCHES.

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