# **5 V Dual Differential PECL** to TTL Translator

#### Description

The MC100ELT23 is a dual differential PECL to TTL translator. Because PECL (Positive ECL) levels are used, only +5 V and ground are required. The small outline 8-lead package and the dual gate design of the ELT23 makes it ideal for applications which require the translation of a clock and a data signal.

The PECL inputs are differential; therefore, the MC100ELT23 can accept any standard differential PECL input referenced from a  $V_{CC}$  of 5.0 V.

#### **Features**

- 3.5 ns Typical Propagation Delay
- 24 mA TTL Outputs
- Flow Through Pinouts
- The 100 Series Contains Temperature Compensation
- Operating Range  $V_{CC} = 4.75 \text{ V}$  to 5.25 V with GND = 0 V
- Internal Input 50 KΩ Pulldown Resistors
- Pb-Free Packages are Available



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#### **MARKING DIAGRAMS\***



SOIC-8 D SUFFIX CASE 751





TSSOP-8 DT SUFFIX CASE 948R





DFN8 MN SUFFIX CASE 506AA



A = Assembly Location

Y = Wafer Lot
Y = Year
W = Work Week
M = Date Code
Pb-Free Package

(Note: Microdot may be in either location)

\*For additional marking information, refer to Application Note AND8002/D.

#### **ORDERING INFORMATION**

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

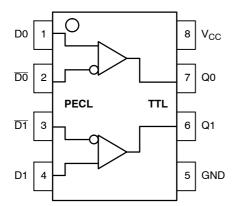


Figure 1. 8-Lead Pinout (Top View) and Logic Diagram

#### **Table 1. PIN DESCRIPTION**

Pin	Function
Qn	TTL Outputs
Dn, Dn	PECL Differential Inputs
V <sub>CC</sub>	Positive Supply
GND	Ground
EP	(DFN8 only) Thermal exposed pad must be connected to a sufficient thermal con- duit. Electrically connect to the most neg- ative supply (GND) or leave unconnec- ted, floating open.

**Table 2. ATTRIBUTES** 

Characte	Value			
Internal Input Pulldown Resistor	50 kΩ			
Internal Input Pullup Resistor		N,	/A	
ESD Protection	. –	kV 00 V		
Moisture Sensitivity, Indefinite Ti	me Out of Drypack (Note 1)	Pb Pkg	Pb-Free Pkg	
	Level 1 Level 1 Level 1	Level 1 Level 3 Level 1		
Flammability Rating	UL 94 V-0	@ 0.125 in		
Transistor Count	91 De	evices		
Meets or exceeds JEDEC Spec	EIA/JESD78 IC Latchup Test			

<sup>1.</sup> For additional information, see Application Note AND8003/D.

**Table 3. MAXIMUM RATINGS** 

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V <sub>CC</sub>	Power Supply	GND = 0 V		7	V
VI	Input Voltage	GND = 0 V	$V_{I} \leq V_{CC}$	0 to 6	V
T <sub>A</sub>	Operating Temperature Range			-40 to +85	°C
T <sub>stg</sub>	Storage Temperature Range			-65 to +150	°C
$\theta_{JA}$	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	SOIC-8 SOIC-8	190 130	°C/W
$\theta_{\sf JC}$	Thermal Resistance (Junction-to-Case)	Standard Board	SOIC-8	41 to 44	°C/W
$\theta_{JA}$	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	TSSOP-8 TSSOP-8	185 140	°C/W
θ <sub>JC</sub>	Thermal Resistance (Junction-to-Case)	Standard Board	TSSOP-8	41 to 44 ± 5%	°C/W
$\theta_{JA}$	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	DFN8 DFN8	129 84	°C/W °C/W
T <sub>sol</sub>	Wave Solder Pb Pb-Free	<2 to 3 sec @ 248°C <2 to 3 sec @ 260°C		265 265	°C
$\theta_{\sf JC}$	Thermal Resistance (Junction-to-Case)	(Note 2)	DFN8	35 to 40	°C/W

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

<sup>2.</sup> JEDEC standard multilayer board - 2S2P (2 signal, 2 power)

Table 4. PECL INPUT DC CHARACTERISTICS V<sub>CC</sub> = 5.0 V; GND = 0.0 V (Note 3)

			-40°C			25°C			85°C		
Symbol	Characteristic	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit
V <sub>IH</sub>	Input HIGH Voltage (Single-Ended) (Note 4)	3835		4120	3835		4120	3835		4120	mV
V <sub>IL</sub>	Input LOW Voltage (Single-Ended)	3190		3525	3190		3525	3190		3525	mV
V <sub>IHCMR</sub>	Input HIGH Voltage Common Mode Range (Differential) (Note 5)	2.2		5.0	2.2		5.0	2.2		5.0	V
I <sub>IH</sub>	Input HIGH Current			255			175			175	μΑ
I <sub>IL</sub>	Input LOW Current	0.5			0.5			0.5			μΑ

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

- 3. Input parameters vary 1:1 with  $V_{CC}.\ V_{CC}$  can vary  $\pm$  0.25 V.
- 4. TTL output  $R_L = 500 \Omega$  to GND.
- 5.  $V_{IHCMR}$  min varies 1:1 with GND,  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$

Table 5. TTL OUTPUT DC CHARACTERISTICS  $V_{CC} = 4.75 \text{ V}$  to 5.25 V;  $T_A = -40 ^{\circ}\text{C}$  to 85  $^{\circ}\text{C}$ 

Symbol	Characteristic	Condition	Min	Тур	Max	Unit
V <sub>OH</sub>	Output HIGH Voltage	I <sub>OH</sub> = -3.0 mA	2.4		(Note 6)	V
V <sub>OL</sub>	Output LOW Voltage	I <sub>OL</sub> = 24 mA			0.5	V
I <sub>CCH</sub>	Power Supply Current			23	33	mA
I <sub>CCL</sub>	Power Supply Current			26	36	mA
Ios	Output Short Circuit Current		-150		-60	mA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

6. Max level is V<sub>CC</sub> – 0.7 V by design.

Table 6. AC CHARACTERISTICS V<sub>CC</sub>= 5.0 V; GND= 0.0 V (Note 7 and Note 8)

			-40°C			25°C			85°C		
Symbol	Characteristic	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit
f <sub>max</sub>	Maximum Toggle Frequency					100					MHz
t <sub>JITTER</sub>	Random Clock Jitter (RMS)					35					ps
t <sub>PLH</sub>	Propagation Delay @ 1.5 V	2.0		5.5	2.0		5.5	2.0		5.5	ns
t <sub>PHL</sub>	Propagation Delay @ 1.5 V	2.0		5.5	2.0		5.5	2.0		5.5	ns
V <sub>PP</sub>	Input Swing (Note 9)	200		1000	200		1000	200		1000	mV
t <sub>r</sub> /t <sub>f</sub>	Output Rise Time (10–90%) Output Fall Time (10–90%)					1.6 1.1					ns ns

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

- 7.  $V_{CC}$  can vary  $\pm$  0.25 V.
- 8. TTL output  $\dot{R}_L$  = 500  $\Omega$  to GND, and  $C_L$  = 20 pF to GND. Refer to Figure 2.
- 9.  $V_{PP}(min)$  is the minimum input swing for which AC parameters are guaranteed. The device has a DC gain of  $\approx 40$ .

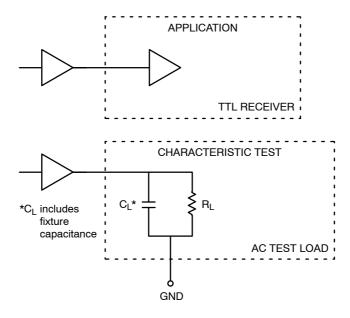


Figure 2. TTL Output Loading Used for Device Evaluation

#### **ORDERING INFORMATION**

Device	Package	Shipping <sup>†</sup>
MC100ELT23D	SOIC-8	98 Units / Rail
MC100ELT23DG	SOIC-8 (Pb-Free)	98 Units / Rail
MC100ELT23DR2	SOIC-8	2500 / Tape & Reel
MC100ELT23DR2G	SOIC-8 (Pb-Free)	2500 / Tape & Reel
MC100ELT23DT	TSSOP-8	100 Units / Rail
MC100ELT23DTG	TSSOP-8 (Pb-Free)	100 Units / Rail
MC100ELT23DTR2	TSSOP-8	2500 / Tape & Reel
MC100ELT23DTR2G	TSSOP-8 (Pb-Free)	2500 / Tape & Reel
MC100ELT23MNR4	DFN8	1000 / Tape & Reel
MC100ELT23MNR4G	DFN8 (Pb-Free)	1000 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

#### **Resource Reference of Application Notes**

AN1405/D - ECL Clock Distribution Techniques

AN1406/D - Designing with PECL (ECL at +5.0 V)

AN1503/D - ECLinPS™ I/O SPiCE Modeling Kit

AN1504/D - Metastability and the ECLinPS Family

AN1568/D - Interfacing Between LVDS and ECL

AN1672/D - The ECL Translator Guide

AND8001/D - Odd Number Counters Design

AND8002/D - Marking and Date Codes

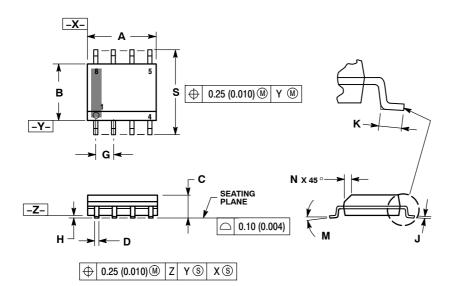
AND8020/D - Termination of ECL Logic Devices

AND8066/D - Interfacing with ECLinPS

AND8090/D - AC Characteristics of ECL Devices

#### PACKAGE DIMENSIONS

#### SOIC-8 NB CASE 751-07 **ISSUE AH**



#### NOTES:

- NOTES:

  1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

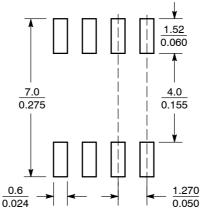
  2. CONTROLLING DIMENSION: MILLIMETER.

  3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.

  4. MAXIMUM MOLD PROTRUSION 0.15 (0.006)
- 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006)
  PER SIDE.
  5. DIMENSION D DOES NOT INCLUDE DAMBAR
  PROTRUSION. ALLOWABLE DAMBAR
  PROTRUSION SHALL BE 0.127 (0.005) TOTAL
  IN EXCESS OF THE D DIMENSION AT
  MAXIMUM MATERIAL CONDITION.
  6. 751–01 THRU 751–06 ARE OBSOLETE. NEW
  STANDARD IS 751, 07
- STANDARD IS 751-07.

	MILLIN	IETERS	INC	HES	
DIM	MIN	MAX	MIN	MAX	
Α	4.80	5.00	0.189	0.197	
В	3.80	4.00	0.150	0.157	
С	1.35	1.75	0.053	0.069	
D	0.33	0.51	0.013	0.020	
G	1.27	7 BSC	0.050 BSC		
Н	0.10	0.25	0.004	0.010	
J	0.19	0.25	0.007	0.010	
K	0.40	1.27	0.016	0.050	
М	0 °	8 °	0 °	8 °	
N	0.25	0.50	0.010	0.020	
S	5.80	6.20	0.228	0.244	

#### **SOLDERING FOOTPRINT\***

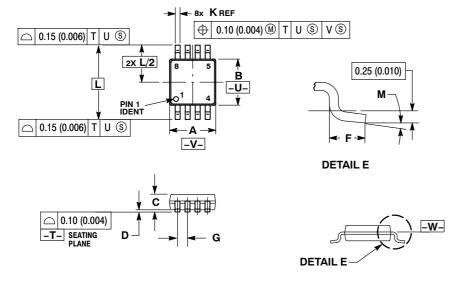


 $\left(\frac{\text{mm}}{\text{inches}}\right)$ SCALE 6:1

<sup>\*</sup>For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

#### **PACKAGE DIMENSIONS**

#### TSSOP-8 **DT SUFFIX** PLASTIC TSSOP PACKAGE CASE 948R-02 **ISSUE A**



- NOTES:
  1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
- 2. CONTINCUING DIMENSION. MILLIDETET.
  3. DIMENSION A DOES NOT INCLUDE MOLD FLASH.
  PROTRUSIONS OR GATE BURRS. MOLD FLASH
  OR GATE BURRS SHALL NOT EXCEED 0.15
- (0.006) PER SIDE.

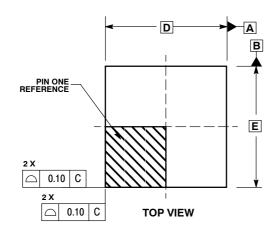
  4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010)
- PER SIDE.

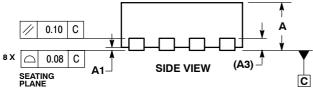
  5. TERMINAL NUMBERS ARE SHOWN FOR
- REFERENCE ONLY.
  6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

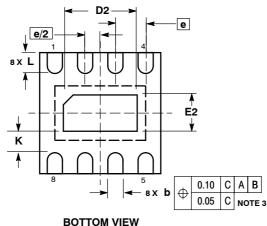
	MILLIN	IETERS	INC	HES
DIM	MIN	MAX	MIN	MAX
Α	2.90	3.10	0.114	0.122
В	2.90	3.10	0.114	0.122
С	0.80	1.10	0.031	0.043
D	0.05	0.15	0.002	0.006
F	0.40	0.70	0.016	0.028
G	0.65	BSC	0.026	BSC
K	0.25	0.40	0.010	0.016
L	4.90	BSC	0.193	BSC
M	0°	6 °	0°	6°

#### PACKAGE DIMENSIONS

#### DFN8 CASE 506AA-01 ISSUE D







- NOTES:
  1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994 . CONTROLLING DIMENSION: MILLIMETERS.
- DIMENSION b APPLIES TO PLATED
  TERMINAL AND IS MEASURED BETWEEN
- 0.25 AND 0.30 MM FROM TERMINAL.
  COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS				
DIM	MIN	MAX			
Α	0.80	1.00			
A1	0.00	0.05			
АЗ	0.20	REF			
b	0.20	0.30			
D	2.00	BSC			
D2	1.10	1.30			
E	2.00	BSC			
E2	0.70	0.90			
е	0.50 BSC				
K	0.20				
L	0.25	0.35			

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