PIC16F87/88

PIC16F87/88 Data Sheet Errata

Clarifications/Corrections to the Data Sheet:

In the Device Data Sheet (DS30487**C**), the following clarifications and corrections should be noted. Any silicon issues related to the PIC16F87/88 will be reported in a separate silicon errata. Please check the Microchip web site for any existing issues.

1. Module: Oscillator Configurations (INTRC and INTOSC)

Summary of Changes

- INTOSC Clock Source
  - The Least Significant bit of the OSCTUNE register – TUN0 (OSCTUNE<0>) – is not implemented.
  - As a result, incrementing or decrementing the OSCTUNE register will not have the expected, single-step change on the INTOSC frequency.
  - When the INTOSC clock source is started, the IOFS bit (OSCCON <2>) is clear, but it becomes set in approximately 100 μs.
  - The INTOSC clock frequency is stable when the IOFS bit is set.
- INTRC Clock Source
  - This 31 kHz, internal RC oscillator source is a separate, fixed frequency. It is not tunable.

These changes result in nine changes, detailed in the clarification:

1. Page 38, Section 4.5.2 – Deletion and modification of some text
2. Page 38, Register 4-1 – Modified some text
3. Page 41, Section 4.6.4 – Deleted and modified text
4. Page 41, Section 4.6.5 – Deleted and modified text
5. Page 42, Table 4-3 – Deleted and modified text
6. Page 43, Section 4.7.1 – Modified some text
7. Page 49, Table 4-4 – Note 1 revised

Change 1. Section 4.5.2

The second paragraph of **Section 4.5.2 "OSCTUNE Register"** is changed as shown.

When the OSCTUNE register is modified, the INTOSC frequency will begin shifting to the new frequency. The INTOSC clock will stabilize within 100 μs. Code execution continues during this shift. There is no indication that the shift has occurred.

Change 2. Register 4-1

The descriptions of bits<5:0> are modified, as highlighted by the change bars.

REGISTER 4-1: OSCTUNE: OSCILLATOR TUNING REGISTER (ADDRESS 90h)

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	TUN5	TUN4	TUN3	TUN2	TUN1	TUN0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **Unimplemented:** Read as '0'

bit 5-1 **TUN<5:1>:** Frequency Tuning bits

01111 = Maximum frequency
01110 =
•
•
•
00001 =
00000 = Center frequency. Oscillator module is running at the calibrated frequency.
11111 =
•
•
•
10000 = Minimum frequency

bit 0 **TUN0:** Placeholder – Bit has no effect on the INTRC frequency. It is provided to enable the OSCTUNE2 register to be incremented and decremented easily.

Change 3. Section 4.6.4

Section 4.6.4 "Modifying the IRCF Bits" is changed as shown.

4.6.4 MODIFYING THE IRCF BITS

The IRCF bits can be modified at any time regardless of which clock source is currently being used as the system clock. The internal oscillator allows users to change the frequency during run time. This is achieved by modifying the IRCF bits in the OSCCON register. The sequence of events that occur after the IRCF bits are modified is dependent upon the initial value of the IRCF bits before they are modified. If the INTRC (31.25 kHz, IRCF<2:0> = 000) is running and the IRCF bits are modified to any other value than '000', the clock source is switched immediately. The IOFS bit (OSCCON<2>) becomes set approximately 100 μs later. Code execution continues while the new frequency stabilizes. Time sensitive code should wait for the IOFS bit to become set before continuing. This bit can be monitored to ensure that the frequency is stable before using the system clock in time critical applications.

If the IRCF bits are modified while the internal oscillator is running at any other frequency than INTRC (31.25 kHz, IRCF<2:0> ≠ 000), the clock source is switched immediately and IOFS remains set.

Change 4. Section 4.6.5

The fourth step of the first of three switching sequences in **Section 4.6.5 "Clock Transition Sequence"** is changed as shown.

4. The IOFS bit is clear to indicate that the clock is unstable. In approximately 100 μs, the IOFS bit will become set, indicating INTOSC is stable. Code execution continues while IOFS is clear.

   Time dependent code should wait for IOFS to become set before continuing.

Change 5. Table 4-3

Table 4-3 is changed as shown, with change bars indicating new or modified text.

TABLE 4-3: OSCILLATOR DELAY EXAMPLES

Clock Switch		Frequency	Oscillator Delay	Comments
From	To			
Sleep/POR	INTRC T1OSC	31.25 kHz 32.768 kHz	CPU Start-up(1)	Following a wake-up from Sleep mode or POR, CPU start-up is invoked to allow the CPU to become ready for code execution.
	INTOSC/ INTOSC Postscaler	125 kHz-8 MHz	100 μs(2) and CPU Start-up(1)	
INTRC/Sleep	EC, RC	DC – 20 MHz		
INTRC (31.25 kHz)	EC, RC	DC – 20 MHz		
Sleep	LP, XT, HS	32.768 kHz-20 MHz	1024 Clock Cycles (OST)	Following a change from INTRC, an OST of 1024 cycles must occur.
INTRC (31.25 kHz)	INTOSC/ INTOSC Postscaler	125 kHz-8 MHz	100 μs(2)	Refer to **Section 4.6.4 "Modifying the IRCF Bits"** for further details.

Note 1: The 5-10 μs start-up delay is based on a 1 MHz system clock.

2: The INTOSC clock source is available immediately and clocks the controller. 100 μs after the INTOSC is enabled (when IOFS becomes set), the INTOSC frequency is stable and meets specifications.

Change 6. Section 4.7.1

The second paragraph in **Section 4.7.1 "RC_RUN Mode"** is changed as shown.

If the system clock does not come from the INTRC (31.25 kHz) when the SCS bits are changed, and the IRCF bits in the OSCCON register are configured for a frequency other than INTRC, the frequency may not be stable immediately. The IOFS bit (OSCCON<2>) will be set when the INTOSC or postscaler frequency is stable, after approximately 100 μs.

Change 7. Table 4-4

The note in Table 4-4 is changed as shown.

TABLE 4-4: CLOCK SWITCHING MODES

Current System Clock	SCS Bits <1:0> Modified to:	Delay	OSTS Bit	IOFS Bit	T1RUN Bit	New System Clock	Comments
LP, XT, HS, T1OSC, EC, RC	10 (INTRC) FOSC<2:0> = LP, XT or HS	8 Clocks of INTRC	0	1 (1)	0	INTRC or INTOSC or INTOSC Postscaler	The internal RC oscillator frequency is dependant upon the IRCF bits.
LP, XT, HS, INTRC, EC, RC	01 (T1OSC) FOSC<2:0> = LP, XT or HS	8 Clocks of T1OSC	0	N/A	1	T1OSC	T1OSCEN bit must be enabled.
INTRC T1OSC	00 FOSC<2:0> = EC or FOSC<2:0> = RC	8 Clocks of EC or RC	1	N/A	0	EC or RC	
INTRC T1OSC	00 FOSC<2:0> = LP, XT, HS	1024 Clocks (OST) + 8 Clocks of LP, XT, HS	1	N/A	0	LP, XT, HS	During the 1024 clocks, program execution is clocked from the secondary oscillator until the primary oscillator becomes stable.
LP, XT, HS	00 (Due to Reset) LP, XT, HS	1024 Clocks (OST)	1	N/A	0	LP, XT, HS	When a Reset occurs, there is no clock transition sequence. Instruction execution and/or peripheral operation is suspended unless Two-Speed Start-up mode is enabled, after which the INTRC will act as the system clock until the OST timer has expired.

Note 1: If the new clock source is the INTOSC or INTOSC postscaler, the IOFS bit will be set approximately 100 μs after the clock change.

REVISION HISTORY

Rev A Document (2/2008)
Original release of this errata. Includes Data Sheet Clarification 1 (Oscillator Configurations, INTRC and INTOSC).

NOTES:

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